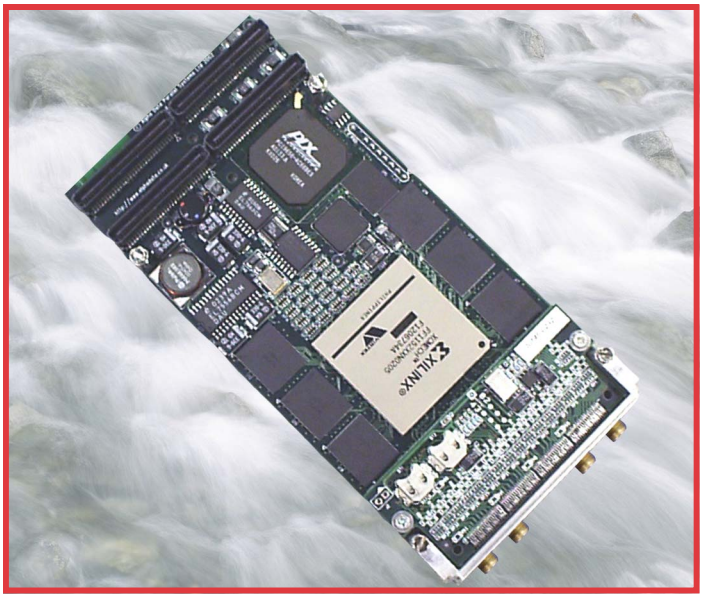
Red River

FlexReceiver Plus PMC

Model 309



- *Industry Standard PMC Form Factor*
- *Dual 14-bit or 12-bit A/D Converters*
- *AC or DC Coupled Analog Inputs*
- *Selectable A/D Sample Clock Frequency*
- *Internal / External Clock and Triggering*
- *Xilinx Virtex-II XC2V3000 to XC2V8000*
- *Data Capture FPGA Function Included*
- *Verilog/VHDL Interface Source Code*
- *Six Banks of 256k/512k/1M x 36 SRAM*
- *PCI Bus Master With Auto DMA Features*
- *32/64-bit and 33/66 MHz PCI Support*
- *Windows / Linux / VxWorks Drivers*

Dual Channel Reconfigurable Digital Receiver

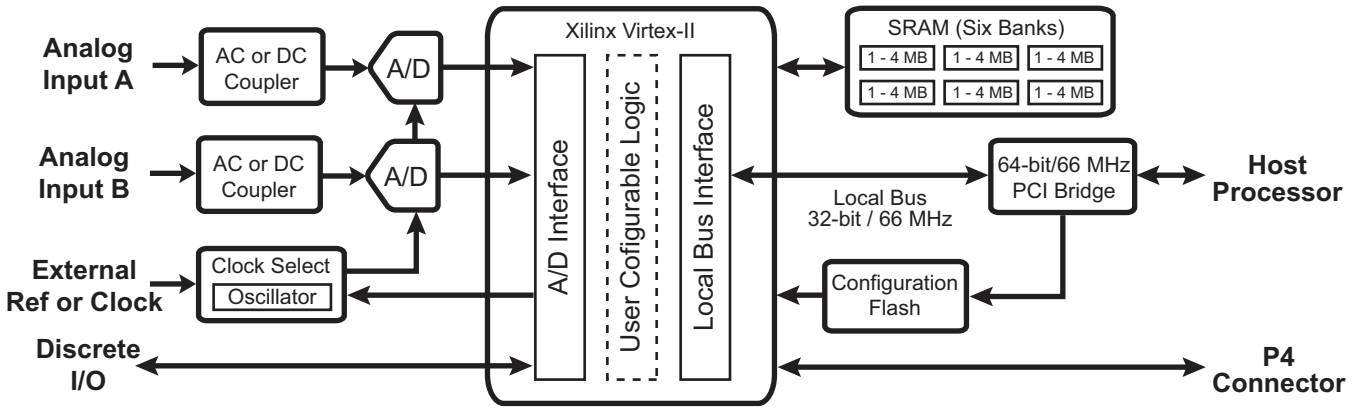
FlexReceiver Plus PMC provides the ideal platform to rapidly field application specific receiver functions minus the expense of custom hardware development. The architecture features a dual channel high performance digitizer tightly coupled to a Xilinx Virtex-II FPGA. The FPGA communicates with the host processor through a dedicated PCI bridge, leaving the majority of the logic uncommitted. Simple interfaces to the digitizer and local bus are easily integrated with user configuration code.

The *FlexReceiver Plus* front-end consists of a dual channel digitizer built from either 14-bit (105 Msps) or 12-bit (210 Msps) A/D converters. The sample clock source is software selectable from either the on-board frequency synthesizer or an external source connected through the front panel. A temperature compensated crystal oscillator is provided as a high stability 10 MHz local reference for the frequency synthesizer. Alternatively, an external reference can be supplied through the front panel to support phase coherent processing among multiple cards.

The analog inputs can be either AC or DC coupled to the A/D converters. The AC coupled configuration supports direct IF sampling (bandpass sampling) of signals up to 200 MHz with only minor impact on performance.

The front panel includes an 8-pin header connected to the FPGA for discrete I/O signals. These can be used to provide triggers to/from external equipment, timing strobes, synchronization signals, or debug ports to assist with FPGA application code development.

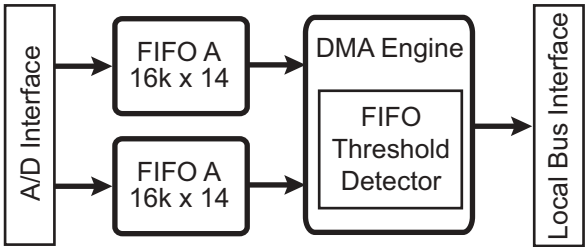
The FPGA is surrounded by six banks of 36-bit SRAM for high speed local data storage. The size of the SRAM is 256 kbytes, 512 kbytes, or 1 Mbyte deep, depending on the build option selected. This memory can be used as a high-speed snapshot recorder to store segments of data without interruption from PCI bus traffic.



Red River Engineering

FlexReceiver Plus PMC

Model 309



Default FPGA Configuration (Dual Channel Signal Acqusition)

The Virtex-II FPGA is supported by a robust set of development tools from Xilinx. Creation of user configuration code follows the standard design flow using a pin assignment file supplied with the *FlexReceiver Plus*. Verilog and VHDL source code for the ADC, SRAM, and local bus interface logic are also provided. Both the FPGA and the configuration PROM can be programmed directly over the PCI bus. The PROM can also be loaded through an optional JTAG connector using the Xilinx iMPACT software.

The *FlexReceiver Plus* product ships with a default configuration preloaded in the PROM to quickly establish communication with the host computer. The card will immediately function as a dual channel signal acquisition unit when power is applied. A software utility is provided to initiate data collection on either or both channels. An internal counter can be used to emulate a signal source in place of the A/D converters to establish a known data pattern.

The signal acquisition function uses the internal BlockRAM resources of the FPGA to provide two 16 ksample FIFOs between the A/D converters and the local bus. Registers are used to set a threshold on each FIFO that will trigger a service request to the DMA engine.

The DMA engine acts as a PCI bus master to initiate data transfers from the FIFO to host memory. A memory destination address, block size, and block count is preloaded by the host prior to each transfer. An interrupt is generated by the FlexReceiver when the final block of the current count has been written.

There are also more sophisticated DMA features available for the signal acquisition function. DMA chaining and scatter-gather techniques are supported by both the hardware and software to optimize data transfer efficiency.

Typical Applications

- Dual Channel Data Acquisition
- Multi-Channel Software Defined Radio Receiver
- Signal Intelligence (SIGINT) Collection
- Receiver Algorithm Prototyping
- Beamforming / TDOA
- Signal Recorder

Specification Summary

Digitizer

Dual AD6645 14-bit A/D Converter Option
- 105 Msps Maximum Sample Rate
- 72 dB Typical SNR (70 MHz AC Coupled)
- 90 dB Typical SFDR (70 MHz AC Coupled)

Dual AD9430 12-bit A/D Converter Option
- 210 Msps Maximum Sample Rate
- 64 dB Typical SNR (70 MHz AC Coupled)
- 70 dB Typical SFDR (70 MHz AC Coupled)

FPGA

- User Configurable Xilinx Virtex-II FPGA
- Verilog/VHDL Interface Source Code
- Default Signal Acquisition Configuration
- Configuration Via PROM or PCI Bus
- Custom Functions Available by Request

Board

- 32/64-bit, 33/66 MHz PCI Compliant
- Universal 5V / 3.3V PCI Signalling
- Bus From FPGA to P4 Connector
- PMC Compliant Physical Format

Options

- XC2V3000 -4, -5, or -6 Speed Grades
- XC2V4000 -4, -5, or -6 Speed Grades
- XC2V6000 -4, -5, or -6 Speed Grades
- XC2V8000 -4, -5, or -6 Speed Grades
- Selectable Oscillator Frequency
- AC or DC Coupled Inputs
- AD6645 or AD9430 A/D Converters
- 6 MB, 12 MB, or 24 MB SRAM

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