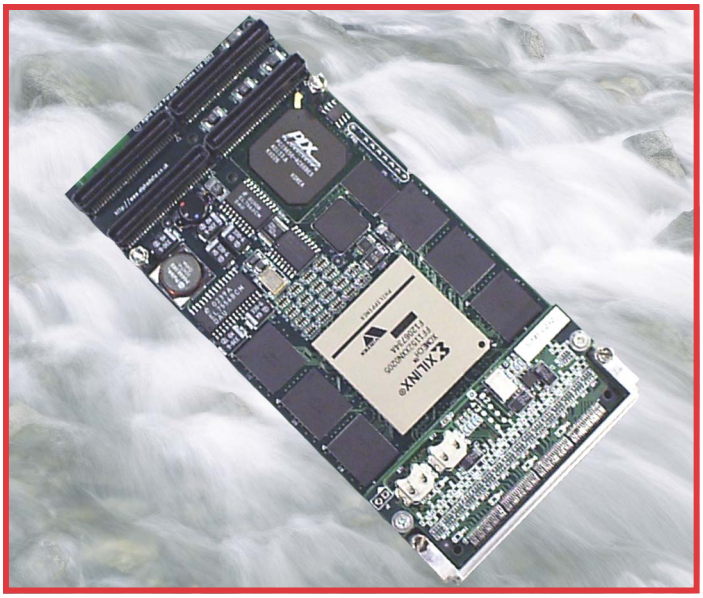
Red River

Sketchboard PMC

Model 305



- *Xilinx Virtex-II XC2V3000 to XC2V8000*
- *Six Banks of 256k/512k x 36 SRAM*
- *Programmable Clock Generator*
- *Interchangeable Front Panel I/O Modules*
- *Wide Selection of I/O Connector Options*
- *DMA Engine FPGA Function Included*
- *Verilog/VHDL Interface Source Code*
- *User Defined P4 Connector I/O Available*
- *PCI Bus Master With Auto DMA Features*
- *32/64-bit and 33/66 MHz PCI Support*
- *Industry Standard PMC Form Factor*
- *Windows / Linux / VxWorks Drivers*

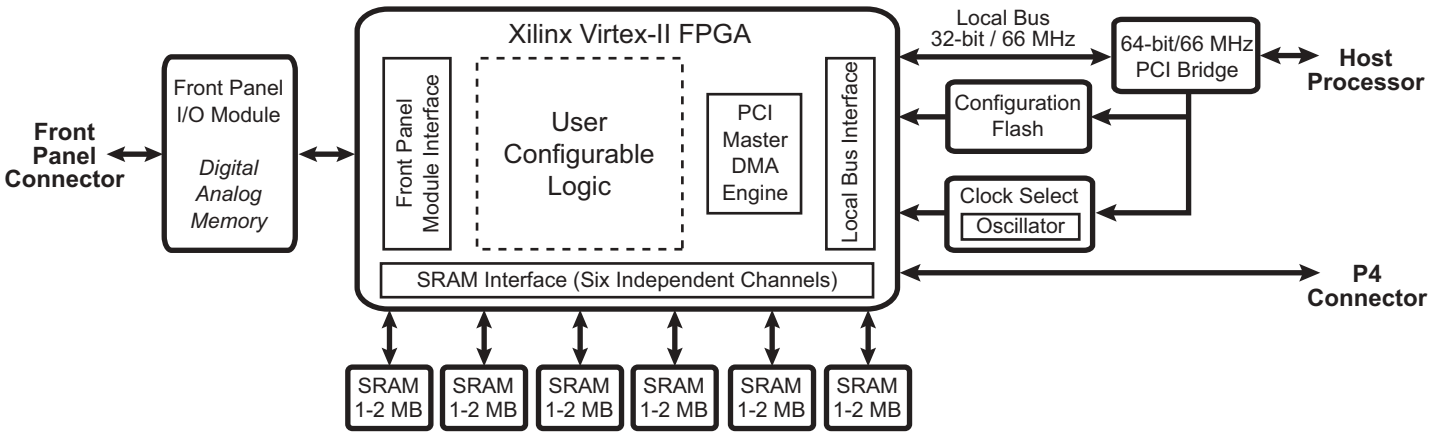
Reconfigurable Logic and I/O

Sketchboard PMC provides the ideal platform to rapidly field application specific logic and I/O functions minus the expense of custom hardware development. The architecture features a Xilinx Virtex-II FPGA tightly coupled to local high-speed SRAM and an interchangeable front panel I/O module. The FPGA communicates with the host processor through a dedicated PCI bridge, leaving the majority of the logic uncommitted. Simple interfaces to the SRAM, front panel module, and local bus are easily integrated with user configuration code.

The *Sketchboard* architecture addresses a wide range of applications by offering flexible logic and I/O configurations. The size and speed of the Virtex-II FPGA is selected as a build option to match device capabilities to the desired performance objectives. The FPGA resources are supplemented by six banks of ZBT SRAM that can be sized from 6 to 12 MBytes. In addition to the standard PCI interface, the FPGA offers a user defined 64-bit datapath to the P4 PMC connector and a 146-bit connection to the front panel I/O module. The I/O module can also be populated with a 128 or 256 MByte DDR SDRAM for additional data storage.

The Virtex-II FPGA is supported by a robust set of development tools from Xilinx. Creation of user configuration code follows the standard design flow using a pin assignment file supplied with the *Sketchboard*. Verilog or VHDL source code for the SRAM, front panel module, and local bus interface logic are also provided. Both the FPGA and the configuration flash memory can be programmed directly over the PCI bus.

The *Sketchboard* can operate as a PCI master to initiate data transfers to/from host memory. A memory destination address, block size, and block count is preloaded by the host into the DMA engine prior to each transfer. An interrupt is generated by the *Sketchboard* when the final block of the current count has been written. DMA chaining and scatter-gather techniques are also supported by both the hardware and software to optimize data transfer efficiency.



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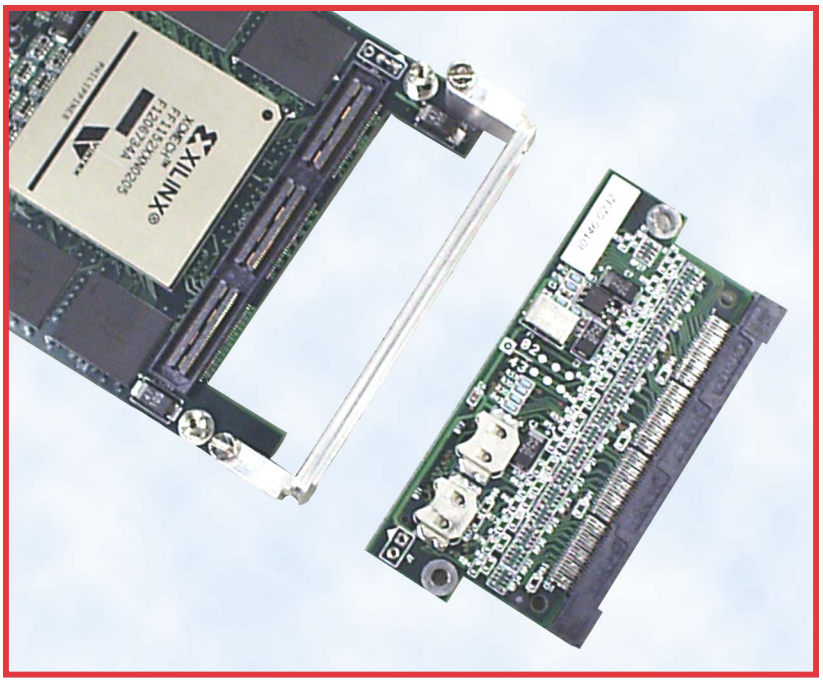

Interchangeable Front Panel I/O Module

There are several interchangeable I/O modules available for *Switchboard* front panel customization. Each module includes a physical connector and the necessary circuitry (i.e. termination resistors) necessary to provide the appropriate electrical interface to the FPGA. The Virtex-II I/O pins are individually programmable for nineteen single-ended or six differential standards including LVDS, LDT, SSTL, and LVPECL. Built-in double data rate I/O registers support LVDS signaling up to 840 Mbps.

Front panel modules with A/D or D/A converters are available to support analog front panel I/O. These modules simplify the development of custom data acquisition or digital radio transceiver functions.

Front panel modules can also increase the memory capacity directly available to the FPGA. A high density DDR SDRAM module supports local storage of large data sets while a ZBT SRAM module supplements the existing high-speed memory.

Typical Applications

- Computation Intensive Algorithm Accelerator
- Multi-Protocol I/O Adapter
- Real-Time Sensor Processing
- High Speed Design Prototyping
- Data Acquisition or Signal Generation
- Software Defined Radio

Specification Summary

FPGA

XC2V3000, 2V4000, 2V6000, or 2V8000
-4, -5, -6 Speed Grade Options
Verilog or VHDL Interface Source Code
PCI Master DMA Engine Function Included
Configuration Via Flash or PCI Bus
Custom Functions Available by Request

SRAM

256k or 512k x 36 ZBT SRAM
Synchronous Operation
Six Independent Channels

Board

32/64-bit, 33/66 MHz PCI Compliant
PLX PCI 9656 Bridge Chip
Universal 5V / 3.3V PCI Signalling
64-bit Bus From FPGA to P4 Connector
ICS9161A Clock Generator Chip
PMC Compliant Physical Format

I/O Options

High Speed Mictor 152-pin (default)
Front Panel Data Port (FPDP) 80-pin
Mini D Ribbon (MDR) 26-pin
SCSI-2 68-pin
DDR SDRAM With Mictor 38-pin
ZBT SRAM With 2 Serial Ports
Dual Channel A/D Converter (SMA or SMB)
Dual Channel D/A Converter (SMA or SMB)

Alpha Data Technology Partner

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