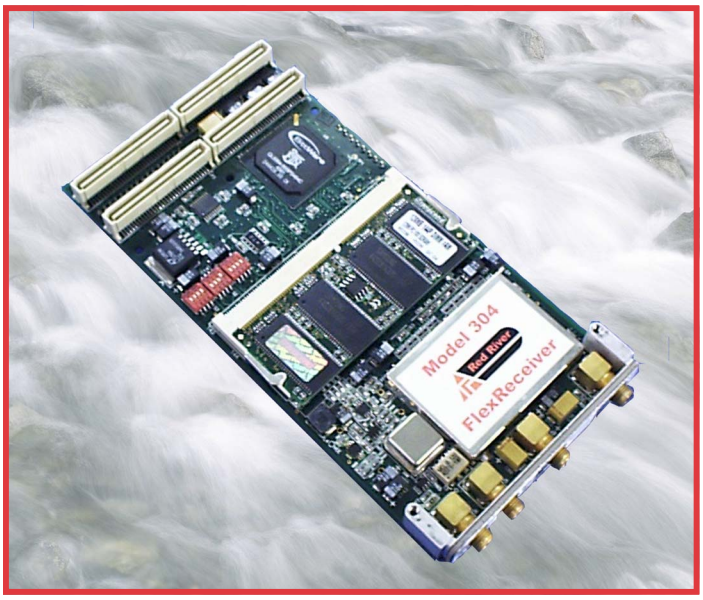
Red River

FlexReceiver PMC

Model 304



- *Dual 14-bit (105 Msps) A/D Converters*
- *AC or DC Coupled Analog Inputs*
- *Selectable A/D Sample Clock Frequency*
- *Internal / External Clock and Triggering*
- *User Programmable XC2V1000 FPGA*
- *Data Capture FPGA Function Included*
- *Verilog/VHDL Interface Source Code*
- *64 - 512 MB SDRAM (144-pin SODIMM)*
- *PCI Bus Master With Auto DMA Features*
- *32/64-bit and 33/66 MHz PCI Support*
- *Industry Standard PMC Form Factor*
- *Windows / Linux / VxWorks Drivers*

Dual Channel Reconfigurable Digital Receiver

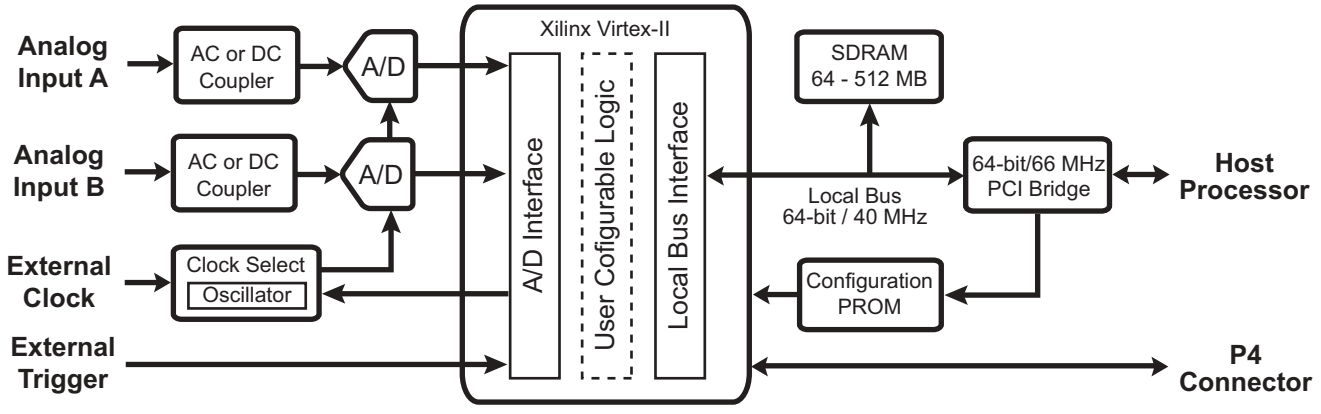
FlexReceiver PMC provides the ideal platform to rapidly field application specific receiver functions minus the expense of custom hardware development. The architecture features a dual channel high performance digitizer tightly coupled to a Xilinx Virtex-II FPGA. The FPGA communicates with the host processor through a dedicated PCI bridge, leaving the majority of the logic uncommitted. Simple interfaces to the digitizer and local bus are easily integrated with user configuration code.

The *FlexReceiver* front-end consists of two Analog Devices AD6645 14-bit A/D converters, each capable of sustained rates up to 105 Msps. The A/D sample clock can be selected from an on-board crystal oscillator or an external source connected through the front panel. A temperature compensated or oven controlled crystal oscillator can be specified as build options to improve on-board clock stability. A programmable clock divider and external trigger available to the FPGA add further flexibility without diminishing clock fidelity.

The analog inputs can be either AC or DC coupled to the A/D converters. The AD6645 supports direct IF sampling (bandpass sampling) of signals up to 200 MHz with only minor impact on performance.

A standard SODIMM socket provides access to a large bank of SDRAM from the local bus. This memory can be used as a high-speed snapshot recorder to store segments of data without interruption from PCI bus traffic.

The Virtex-II FPGA is supported by a robust set of development tools from Xilinx. Creation of user configuration code follows the standard design flow using a pin assignment file supplied with the *FlexReceiver*. Verilog and VHDL source code for the A/D and local bus interface logic are also provided. Both the FPGA and the configuration PROM can be programmed directly over the PCI bus. The PROM can also be loaded through an optional JTAG connector using the Xilinx iMPACT software.



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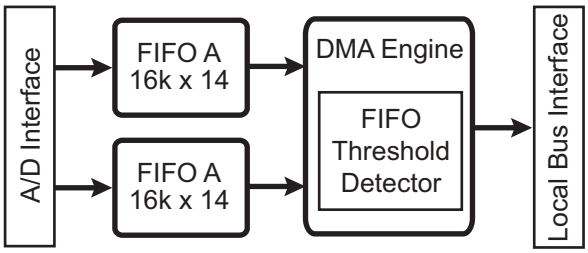
Model 304



Default FPGA Configuration (Dual Channel Signal Acqusition)

The *FlexReceiver* product ships with a default configuration preloaded in the PROM to quickly establish communication with the host computer. The card will immediately function as a dual channel signal acquisition unit when power is applied. A software utility is provided to initiate data collection on either or both channels. An internal counter can be used to emulate a signal source in place of the A/D converters to establish a known data pattern.

The signal acquisition function uses the internal BlockRAM resources of the FPGA to provide two 16 ksample FIFOs between the A/D converters and the local bus. Registers are used to set a threshold on each FIFO that will trigger a service request to the DMA engine.

The DMA engine acts as a PCI bus master to initiate data transfers from the FIFO to host memory. A memory destination address, block size, and block count is preloaded by the host prior to each transfer. An interrupt is generated by the FlexReceiver when the final block of the current count has been written.

There are also more sophisticated DMA features available for the signal acquisition function. DMA chaining and scatter-gather techniques are supported by both the hardware and software to optimize data transfer efficiency.

Typical Applications

- *Dual Channel Data Acquisition*
- *Multi-Channel Software Defined Radio Receiver*
- *Signal Intelligence (SIGINT) Collection*
- *Receiver Algorithm Prototyping*
- *Beamforming / TDOA*
- *Signal Recorder*

Specification Summary

Digitizer

Two AD6645 14-bit A/D Converters
105 Msps Maximum Sample Rate
AC or DC Coupled Inputs
64 dB Min SNR (15 MHz Input/105 Msps)
77 dB Min SFDR (15 MHz Input/105 Msps)

FPGA

User Configurable Xilinx Virtex-II FPGA
Verilog/VHDL Interface Source Code
Default Signal Acquisition Configuration
Configuration Via PROM or PCI Bus
Custom Functions Available by Request

Board

144-pin SODIMM Memory Socket
32/64-bit, 33/66 MHz PCI Compliant
Universal 5V / 3.3V PCI Signalling
Bus From FPGA to P4 Connector
PMC Compliant Physical Format

Options

SMA or SMB Analog Input Connectors
XC2V250 -4, -5, or -6 Speed Grades
XC2V500 -4, -5, or -6 Speed Grades
XC2V1000 -4, -5, or -6 Speed Grades
XO, TCX, OCXO Crystal Oscillators
Selectable Oscillator Frequency
80 or 105 Msps AD6645 Speed Grade
64, 128, 256, or 512 MB SDRAM

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