- ▲ *Industry Standard CPCI Form Factor*
- ▲ *Baseband or 70 MHz IF Analog Interface*
- ▲ *40 MHz Analog I/O Bandwidth*
- ▲ *8.6 MHz Maximum Signal Bandwidth*
- ▲ *Up to 8 Channels on PMC or PCI*
- ▲ *Up to 16 Channels on CPCI or VME*
- ▲ *Up to 90 dB Linear Dynamic Range*
- ▲ *TDMA Event Scheduler and Time Tagging*
- ▲ *PCI Bus Master With Auto DMA Feature*
- ▲ *32/64-bit and 33/66 MHz PCI Support*
- ▲ *Front Panel Control for Synchronization*
- ▲ *Includes Waveformer Configuration Tool*
- ▲ *Windows / Linux / VxWorks Drivers*

PolyChannel Programmable Digital Receiver

Channel Surfer CPCI transforms any computer into a high performance software defined radio receiver. The unique polychannel architecture combines the flexibility, performance, and precision of advanced digital downconverter chips with a modern analog IF front-end to address both narrowband and wideband applications. The industry standard PCI interface simplifies programming and eases the transition from a desktop development environment to an embedded target platform. The Model 206 provides up to eight channels in a 3U form factor. The model 207 is a 6U card that can be configured for either eight or sixteen channel operation.
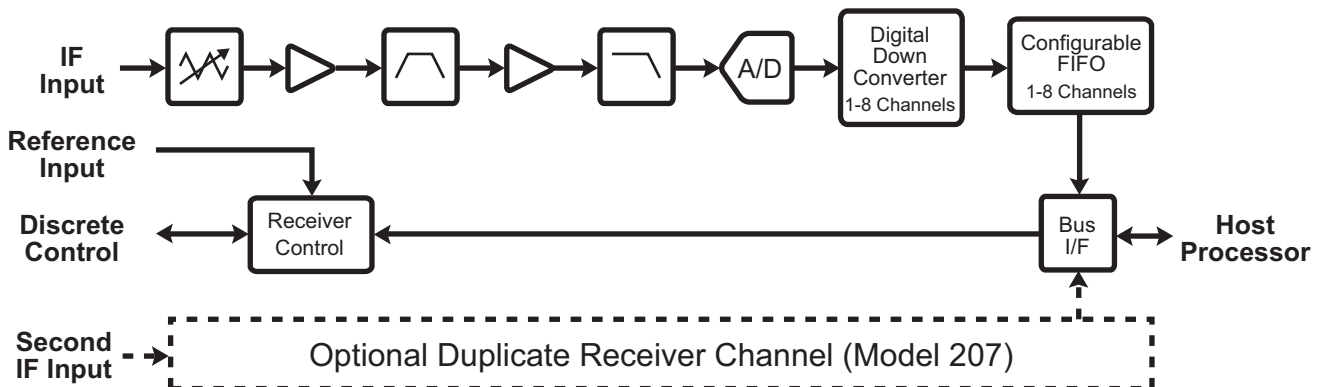
The receiver accepts an analog IF input through an SMB connector located on the front panel. The signal is routed through a digitally controlled attenuator and buffer amplifier immediately preceding the analog anti-alias filter. A second amplifier stage boosts the signal to match the input range of the A/D converter.
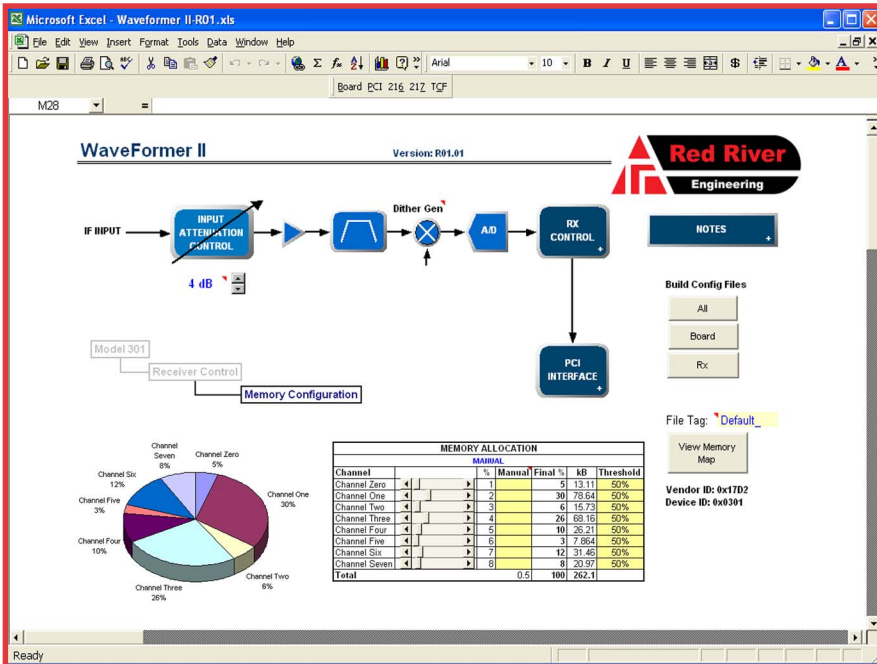
Samples out of the A/D converter are passed to a digital downconverter that can produce from one to eight independent output channels. The maximum signal bandwidth available in each channel increases as the number of channels is reduced. Each channel tunes to a signal of interest and performs amplitude adjustment based on gain control settings.

The complex data samples produced by the downconverter are stored in a configurable FIFO. The FIFO organization can be matched to the number of active output channels. The depth of each FIFO is also variable, allowing higher sample rate channels to obtain more memory.

Channel Surfer can operate as either a bus master or target, allowing DMA transfers to be initiated either autonomously by the receiver or under direct control of the host. Each FIFO is assigned a programmable threshold that signals either the local controller or the host for service.

The Waveformer configuration tool simplifies receiver programming.

Channel Surfer offers a simple memory-mapped host interface referenced to a single base address. The host processor has direct access to all control registers, including the receiver input attenuator level, FIFO memory allocation by channel, downconverter (ISL5216) configuration space, local command/ status, and receiver data flow control. The interface includes an interrupt to alert the host of an error condition or data service request.

Channel Surfer programming is simplified by the *Waveformer* configuration tool that automates the process of computing register values based on the desired performance characteristics of the receiver. The user enters configuration information through a series of menu-driven spreadsheets that accept input based on available register options. The spreadsheets also perform error checking to eliminate configuration conflicts and graphically display key performance parameters in simple block diagrams and frequency response plots. The configuration tool generates a file containing the complete memory map that can be easily uploaded from the host.

Typical Applications

▲ *Signal Intelligence (SIGINT) Collection*

▲ *Beamforming / TDOA (Smart Antenna, E911)*

▲ *Multi-Mode Software Defined Radio Receiver*

▲ *Multi-Channel Narrowband Digital Receiver*

▲ *Single Channel Wideband Digital Receiver*

▲ *Signal Recorder*

Specification Summary

▲ *Receiver*

Baseband or 70 MHz IF (40 MHz BW)
-12 dBm Input Power (Full Scale)
0 dBm 3rd Order Intercept Point
20 dB Analog Gain Control
14-bit, 93 MSPS A/D Converter
Intersil ISL5216 Downconverter
23.2 MSPS Max Complex Output
1-8 Independent Output Channels
256 kbyte Configurable Data FIFO
8.6 MHz Maximum Signal Bandwidth
   (Single Channel Operation)
2 MHz Maximum Signal Bandwidth
   (Eight Channel Operation)
96 dB Digital Automatic Gain Control
>90 dB Linear Dynamic Range (100 kHz)

▲ *Board*

32/64-bit, 33/66 MHz PCI Bus
Multi-Channel Auto DMA Engine
Precision TDMA Event Scheduler
Precision Time Tagging
10 MHz 3 ppm Local Reference
5 to 25 MHz Reference Input

▲ *Options*

Model 207 - One or Two Transceivers
Customization Available by Request

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