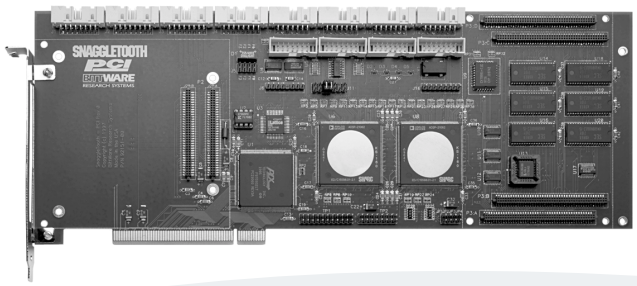
Snaggletooth-PCI

Dual Processor ADSP-2106x PCI Board



SHARC® Power on Industry-Standard PCI Bus

The Snaggletooth-PCI combines power with speed and flexibility. Its two Analog Devices ADSP-2106x SHARC DSPs give it the power of the world's fastest digital signal processors, while the industry-standard PCI bus adds speed and performance. A BITSI mezzanine site for off-the-shelf I/O interfaces and a SHARCPAC™ interface for adding processor and memory expansion modules complete the package with amazing flexibility.

Data Streaming

The two SHARC DSPs share a common processor bus, which allows them to access an optional bank of up to 512K x 48 bits of external SRAM, I/O devices on a BITSI mezzanine, the SHARCPAC interface, and the internal SRAM of the other SHARC processor. Eight external link ports and four external serial ports allow external devices to communicate with the processors.

PCI Interface

The bus-mastering-capable PCI bus interface gives host computers direct access to the SHARC processors' IOP registers and their internal dual-ported SRAM, allowing the host to reset and boot the SHARC processors, load program images, and examine memory. The PCI interface also has direct access to the shared bank of external SRAM and the SHARCPAC interface.

I/O Interface

Using the link ports, serial ports, and a 32-bit-wide data bus, the BITSI I/O mezzanine interface can perform optimized I/O transfers with the SHARC processors. With BittWare's large selection of BITSI I/O mezzanines, you have a variety of options to help you solve your I/O requirements.

Processor and Memory Expansion

The SHARCPAC expansion site allows you to add processor or memory expansion mezzanines to the Snaggletooth-PCI. You can easily reconfigure the Snaggletooth-PCI to match your multiprocessing and memory requirements. The SHARCPAC interface's link and serial ports allow it to communicate with the Snaggletooth-PCI SHARC processors, devices on the BITSI mezzanine, and other link-port-compatible devices.

Available Development Tools

BittWare offers a complete software development kit that allows you to easily integrate the Snaggletooth-PCI into your system. The software tools include a comprehensive host interface library, a standard I/O library, and diagnostic utilities. The board is also fully compatible with Analog Devices' VisualDSP® software development tools, and it supports in-circuit emulation

Features

- Two ADSP-2106x SHARC DSPs running at 40MHz
- Up to 512K x 48 zero-wait-state external SRAM
- SHARC-processor-optimized high-performance BITSI I/O mezzanine site
- Eight external link ports (up to 40 MB/s each)
- Four external serial ports (up to 40 Mb/s each)
- PCI interface for direct, high-speed master/slave access to both SHARC DSPs and external memory
- Supports in-circuit emulation
- Complete development tools available

BittWare

Specifications

BOARD ARCHITECTURE

Processors
- Two 40 MHz Analog Devices ADSP-2106x SHARC DSPs

External Memory
- Up to 512K x 48 bits (3 MB) zero-wait-state SRAM shared by both SHARC processors in addition to the SHARC processors' internal SRAM

Link Ports
- Six links per on-board processor
- Eight external link ports from on-board processors and four from the SHARCPAC interface

Serial Ports
- Two serial ports per on-board processor
- Four external serial ports connected to on-board processors (two from each processor)

PCI Interface
- Provides 32-bit master/slave (132 MB/s peak transfer rate) access to the SHARC processors
- All internal SHARC processor memory, IOP registers, and external memory are mapped to PCI memory space
- Supports hardware interrupts in both directions and host-based booting of SHARC processors

I/O Interface
- The BITSI Rev. 2 mezzanine site supports four SHARC link ports, three serial ports, and a 32-bit data bus
- SHARCPAC Rev. 1.2 module site supports sixteen link ports, three serial ports, interrupts, flags, and access to SHARC processor bus
- SHARCPAC modules can expand program and data memory, add multiple processors, or supply custom I/O interfaces

Debug Port
- 14-pin IDC header for IEEE JTAG 1149.1 boundary scan with extensions for in-circuit emulation
- Supports White Mountain DSP ICE emulators

Power
- 5V @ 1.5 A typical, 2.5 A max (not including optional BITSI mezzanine)

Size
- 12.283" x 4.5" (4.825" including edge connector)

ADSP-2106x SHARC DSPs

Processing Rate
- 40 MHz, 25 ns instruction rate, 120 MFLOPS, 40 MIPS

Arithmetic
- 32/40-bit floating point, 32-bit integer

On-Chip Memory
- 2/4 Mbits (21062/21060) dual-ported SRAM organized ×32 or ×48

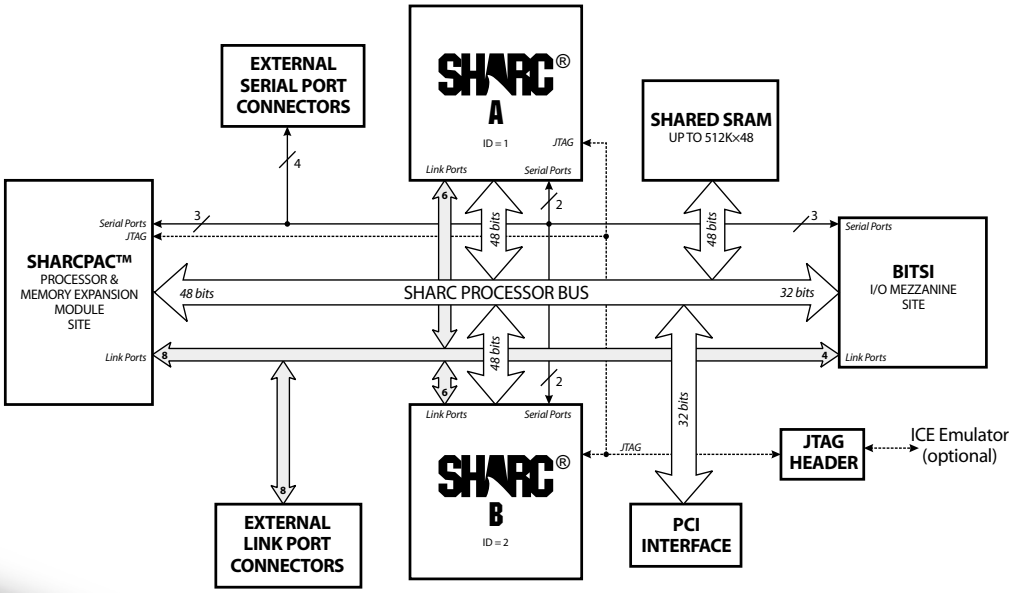
Off-Chip Addressing
- 4 Gigawords addressable memory space
- Memory addressable as 16-, 32-, 40-, or 48-bit words
- Programmable wait-state generation

I/O
- Integrated I/O processor with ten-channel DMA controller, six 40 MB/s link ports, and two 40 Mb/s serial ports

SOFTWARE SUPPORT

Host Interface
- BittWare's software development kit for Windows 95®, Windows 98, and Windows NT contains a C-callable library of board control and communications routines
- Porting kit available for other operating system platforms
- Linux port available

Development Tools
- Analog Devices VDSP tools include C compiler, assembler, linker, simulator, and source code debugger
- Eonic Systems' Virtuoso™ operating system



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