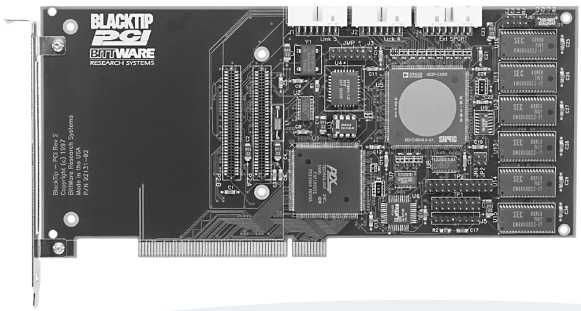
Blacktip-PCI

Single Processor ADSP-2106x PCI Board



SHARC Processing on PCI Bus Platform

BittWare has combined the features of the popular Blacktip-ISA board with the punch of the PCI host bus interface to bring you the Blacktip-PCI. We packed a high-performance Analog Devices ADSP-2106x SHARC DSP, up to 512K words × 48 bits of zero-wait-state SRAM, and a BITSI I/O mezzanine site into a single board for the PCI bus platform.

External Memory

Connected to a 48-bit external processor bus, the SHARC processor has direct access to the optional bank of SRAM and to memory-mapped I/O devices on the BITSI mezzanine. The PCI interface also has direct access to the bank of SRAM and the SHARC processor's internal dual-ported memory.

PCI Interface

The bus-mastering-capable PCI bus interface gives host computers direct access to the SHARC processor's IOP registers and its internal dual-ported SRAM, allowing the host to reset and boot the SHARC processor, load program images, and examine memory. The PCI interface also has direct access to the bank of external SRAM.

I/O Interface

Using the link ports, serial ports, and 32-bit-wide data bus on the Blacktip-PCI's I/O interface, a BITSI I/O mezzanine can perform optimized I/O transfers with the SHARC processor. With BittWare's large selection of BITSI I/O mezzanines, you have a variety of options for exchanging real-world signals with the SHARC processor.

Data Streaming

The SHARC processor can use its external link port connectors to communicate directly with other SHARC processors within the PC or in other systems. Four additional link ports connect to the BITSI mezzanine, allowing high-performance data streaming between the BITSI and the SHARC processor. The Blacktip-PCI SHARC processor can also access serial devices on the BITSI using its two serial ports.

Available Development Tools

BittWare offers a complete software development kit that allows you to easily integrate the Blacktip-PCI into your system. The software tools include a comprehensive host interface library, a standard I/O library, and diagnostic utilities. The board is also fully compatible with Analog Devices' VisualDSP® software development tools, and it supports in-circuit emulation.

Features

- One ADSP-2106x SHARC® DSP running at 40 MHz
- Up to 512K × 48 optional external SRAM
- High-speed PCI bus interface
- Supports in-circuit emulation
- SHARC processor-optimized high-performance BITSI I/O mezzanine site
- Two external link ports (up to 40 MB/s)
- Complete development tools available

BittWare

Specifications

BOARD ARCHITECTURE

Processor
- One 40 MHz ADSP-2106x SHARC DSP
- External SHARC processor bus provides fast memory access and direct data transfers to and from the BITSI interface

External Memory
- Optional external SRAM with zero-wait-state access
- Available in 128K or 512K depths, 32 or 48 bits wide

Link Ports
- Two external links connect directly to the SHARC processor
- Four links provide high-performance data paths from the SHARC processor to the BITSI I/O mezzanine interface

Serial Ports
- Two serial ports are routed to the BITSI I/O mezzanine interface:
  - One serial port is configurable for either a standard two-way connection or a two-wire TDM connection to the BITSI interface
  - One serial port is configurable for either a standard two-way connection to the BITSI interface or to an external connector

PCI Interface
- 32-bit access to the SHARC processor's IOP registers and all internal SRAM
- Direct 32-bit access to external SRAM
- Supports hardware interrupts in both directions

I/O Interface
- The BITSI mezzanine site supports four SHARC link ports, three serial ports, and a 32-bit data bus

Debug Port
- 14-pin IDC header for IEEE JTAG 1149.1 boundary scan with extensions for in-circuit emulation
- Supports White Mountain DSP ICE emulators

Power
- 1A @ 5V typical (not including optional BITSI mezzanine)

Size
- 8.9" × 4.2" (including fingers) PCI bus format

ADSP-2106x SHARC DSP PROCESSOR

Processing Rate
- 40 MHz, 25 ns instruction rate, 120 MFLOPS, 40 MIPS

Arithmetic
- 32/40-bit floating point, 32-bit integer

On-Chip Memory
- 2/4 Mbits (21062/21060) dual-ported SRAM organized ×32 or ×48

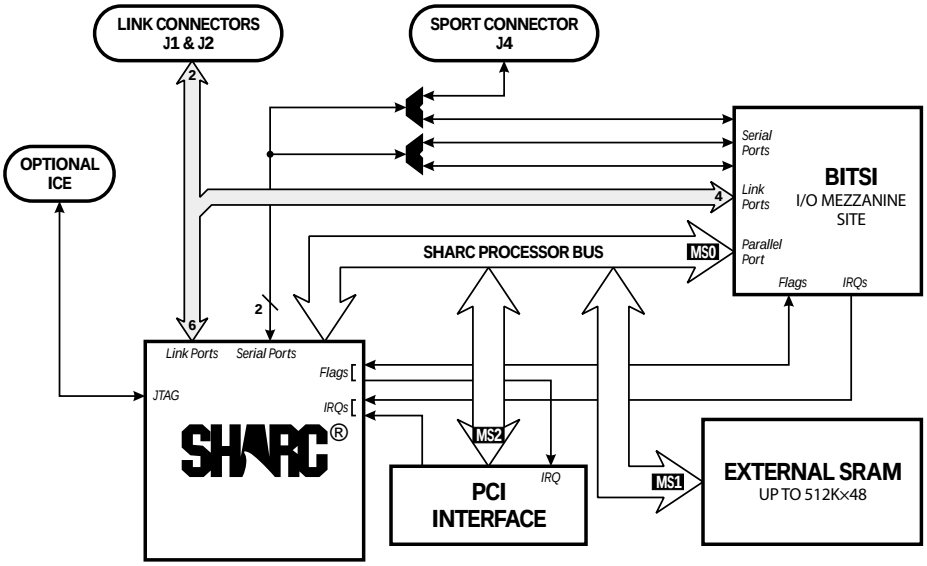
Off-Chip Addressing
- 4 Gigawords addressable memory space
- Memory addressable as 16-, 32-, 40-, or 48-bit words
- Programmable wait-state generation

I/O
- Integrated I/O processor with ten-channel DMA controller, six 40 MB/s link ports, and two 40 Mb/s serial ports

SOFTWARE SUPPORT

Host Interface
- The DSP21k Toolkit for Windows 95® and Windows NT contains a C-callable library of board control and communications routines
- Porting kit available for other operating system platforms
- Linux port available

Development Tools
- Analog Devices ANSI C compiler, assembler, linker, simulator, and source code debugger



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