DDR-bitsi/104

PC/104 BITSI I/O Mezzanine with 4-Channel Digital Down Converter

The DDR-bitsi/104 is a digital drop receiver with four independent digital down conversion channels. It interfaces to ADSP-2106x SHARC processors on BittWare's PC/104 form-factor host boards that have a bitsi/104 interface. Featuring the Graychip GC4014 4-channel Digital Down Converter, the Analog Devices AD6644 A/D converter, and an optional oven-controlled crystal oscillator (OCXO) and word clock, the DDR-bitsi/104 is a powerful high-accuracy I/O component for your software radio application.

Quad Digital Receiver

Graychip's GC4014 distributes digitized IF data to either four real input or two complex input down-convert channels at input rates up to 64 MSPS. It features independent tuning frequencies and phase/gain controls and provides programmable decimation. The Graychip GC4014 also supports frequency tuning from as wide as 4 MHz to as narrow as 1 kHz.

A/D Converter

The DDR-bitsi/104 is populated with Analog Devices' AD6644 14-bit, 65 MSPS A/D converter. It features a 100 dB multi-tone SFDR, and a 74 dB SNR. The converter is designed to target multi-channel, multi-mode receivers, and when coupled with the Graychip GC4014 Digital Down Converter, it represents a powerful component in the software radio chain.

Automatic Gain Controller

The DDR-bitsi/104 features the DAC-8562, a 12-bit, 1 MSPS D/A converter from Analog Devices. The DAC-8562 provides an automatic gain control (AGC) feedback loop that can be used to control receiver front-end electronics.

bitsi/104 Interface

The DDR-bitsi/104 is a bitsi/104 format board, which allows you to connect it to a PC/104 format host board that has a bitsi/104 connector. The bitsi/104 interface provides a serial TDM bus and a parallel bus. The serial TDM bus moves data from the DDC, and the parallel bus moves raw sampled spectrum data from the FIFO. The parallel bus is used for programming the Graychip DDC and the controller.

FIFO Snapshot Buffer

An optional 256K, zero-wait-state FIFO is provided on-board to allow you to view and assess unprocessed data on a snapshot basis.

High-Accuracy, High-Stability Clocking

An optional on-board OCXO of 59.535 MHz is available to replace the standard crystal oscillator. The OCXO is specified with frequency trimming to within +/- 0.1 ppm, frequency stability of +/- 2.5 ppm over –40 to +85 ºC, +/- 0.3 ppm for a +/- 5% variation in power supply, and +/-1 ppm per year aging. When either crystal is the source of the clock, it generates an output word clock of 44.1 KHz with a TTL level, 50-Ohm drive.

Features

- Graychip, Inc. GC4014 quad Digital Down Converter (DDC)
  - Four independent down converters
  - Frequency tuning as wide as 4 MHz and as narrow as 1 kHz
- Analog Devices AD6644 100 dB multi-tone SFDR, 14-bit, 65 MSPS A/D converter
- Automatic Gain Control output
- bitsi/104 interface to Analog Devices' SHARC DSPs
- Optional 256K on-board FIFO for snapshot spectrum analysis
- Optional high-stability and low-aging OCXO clock source
- 50 Ohm clock output driver for audio word clock

BittWare

Specifications

BOARD ARCHITECTURE

A/D Converter
- 14-bit, 65 MSPS conversion rate
- 100 dB multi-tone SFDR
- Sampling jitter of < 300 fs
- 74 dB SNR

Automatic Gain Control Output
- 12-bit, 1 MSPS Digital to Analog Converter
- Vout: 0 to 4.096V
- +/- 5mA drive
- One pole low-pass at 1.5MHz on output

Quad Digital Receiver
- Input rates up to 64 MSPS
- Four real input or two complex input down-convert channels
- Independent tuning frequencies and phase/gain controls
- Decimation factors of 16 to 32,768 real or 32 to 65,536 complex
- 0.02 Hz tuning resolution
- 0.14 dB gain resolution
- < 0.05 dB pp passband ripple
- > 100 dB far image rejection
- > 95 db SFDR
- 63 tap FIR output filter
- Nyquist filtering for QPSK or QAM symbol data

256K x 18 FIFO
- 256K x 18 bit
- IDT standard mode
- Snapshot capture based on FIFO full flag
- Read rates at 0 wait state (33/40 MHz)

Optional OCXO and Word Clock
- 59.535 MHz on-board oscillator or external clock
- Frequency accuracy to within +/- 0.1 ppm
- Frequency stability of +/- 2.5 ppm over -40 to +85 ºC
- +/- 0.3 ppm for a +/- 5% variation in power supply
- +/-1 ppm per year aging
- 44.1 KHz, TTL level with 50 Ohm drive

bitsi/104 Interface
- Allows down-converted (channelized) data to be DMA'd directly to one of the host PC/104 SHARC processors' local memory via the TDM serial bus

Clocking Options
- Standard oscillator
- On-board OCXO
- External clock source
  - Single-ended or differential input
  - 10 dBm into 100 W (sine wave or square)

Power Requirements
- +5V @ 350mA (typical)
- +3.3V @ 700mA (typical)
- 4.06 W Total (typical)

Size
- 3.6" x 3.8" PC-104 Plus format

SOFTWARE SUPPORT

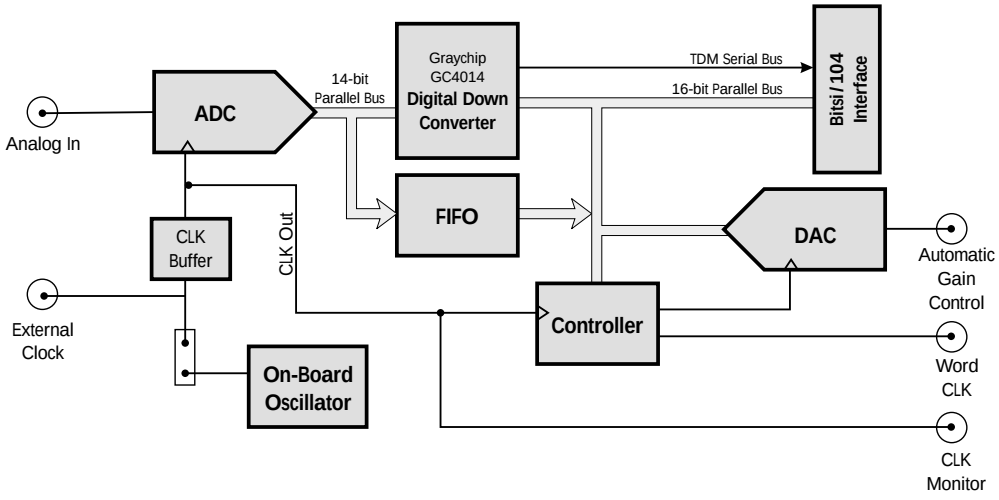
Host Interface
- BittWare's software development kit for Windows® 95/98/NT/2000 is a C library of board control and communications routines
- Porting kit available for other operating systems

Development Tools
- Analog Devices' VisualDSP tools include a C compiler, assembler, linker, simulator, and debugger
- BittWare SHARC LAB interface to MATLAB Simulink® and Real-Time Workshop®
- BittWare SpeedDSP function library

Ordering Information

DDB4-00-XY

X=FIFO	Y=Clock
0= No FIFO	0= Standard oscillator
6= 256K FIFO	1= OCXO



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