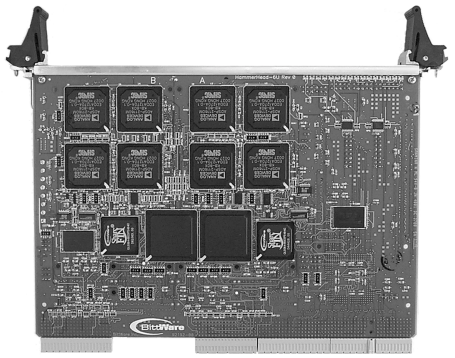
HH6U: Hammerhead-6U-cPCI

Eight ADSP-21160 64-bit, 66 MHz 6U cPCI Board



Eight ADSP-21160s on CompactPCI Form Factor

BittWare's Hammerhead-6U-cPCI board packs the processing power of eight ADSP-21160 SHARC® DSPs and the speed of a 64-bit, 66 MHz PCI interface on a 6U CompactPCI board. Along with the eight Analog Devices' ADSP-21160 processors, the board also features up to three banks of SDRAM, two 2 MB banks of FLASH RAM, and two PMC+ sites.

SharcFIN ASIC for SHARC DSPs

The Hammerhead-6U-cPCI incorporates a BittWare SharcFIN ASIC for each DSP cluster. The SharcFIN ASICs flexibly interface the ADSP-21160 DSPs to the 64-bit, 66 MHz PCI bus, the SDRAM, the FLASH memory, and a peripheral bus. They also provide a feature-rich set of DMA functions and interrupt options to support very high-speed, real-time data flow with minimum processor overhead.

ADSP-21160 DSPs

The Hammerhead-6U-cPCI is configured with eight 100 MHz ADSP-21160 DSPs, arranged in two clusters of four processors. The ADSP-21160 processors are code-compatible with the ADSP-2106x SHARC DSPs, making it easier to integrate existing code. Each cluster of four ADSP-21160 processors shares a common 50 MHz, 64-bit cluster bus, which gives them access to the board's SDRAM, the PCI bus interface, and the other three SHARC processors. For additional I/O, each processor also has four flags, three interrupts, six link ports, and two serial ports. Each DSP also features 4 Mb of on-chip, dual-ported SRAM.

PMC+ Mezzanine Sites

The Hammerhead-6U-cPCI features a PMC+ site for each cluster. The PMC+ (PCI Mezzanine Card) sites have front-panel access and allow you to attach standard PMC modules to the board, adding I/O or additional processors and memory. The PMC+ sites also function as proprietary interfaces that allow you to attach BittWare's PMC+ I/O modules for low-latency, high-performance I/O via four 100 MB/s link ports and a 50 Mb/s TDM serial port from each mezzanine site.

Available Development Tools

BittWare offers a complete software development kit that allows you to easily develop application code and integrate the Hammerhead-6U-cPCI into your system. The software tools include a comprehensive host interface library (HIL), a standard I/O library, and diagnostic utilities. The board is fully compatible with Analog Devices' VisualDSP® code development tools and supports in-circuit emulation. It is also compatible with SpeedDSP, BittWare's highly-optimized C-callable runtime libraries, and with SharcLAB, BittWare's interface to MATLAB Simulink® and Real-Time Workshop®.

Features

- Eight ADSP-21160 SHARC DSPs (two clusters of four DSPs each) running at 100 MHz (4800 MFLOPS)
- 64-bit, 66 MHz CompactPCI interface
- Three banks (1 per cluster and 1 optional shared) of 64–512 MB SDRAM modules (standard 144-pin SODIMMs)
- Two PMC+ mezzanine sites for standard PMC modules or for proprietary PMC+ I/O modules
- Eight 100 MB/s link ports and two 50 Mb/s serial TDM buses for access between DSP clusters and PMC+ sites
- Eight rear-panel link ports and two rear-panel TDM serial ports
- Two dual UARTs provide two RS-232s per cluster (one to rear panel, one to front panel)
- Two 2 MB banks of FLASH RAM

BittWare

Specifications

BOARD ARCHITECTURE

Processors

- Eight Analog Devices ADSP-21160 SHARC DSPs, arranged as two clusters of four
- 600 MFLOPs per DSP
- 4 Mb of on-chip dual-ported SRAM per DSP
- Integrated I/O processor with fourteen-channel DMA controller, six 100 Mbyte/sec link ports, and two 100 Mbit/sec serial ports

External Memory

- 2 banks (one per cluster) 64-512 MB SDRAM (standard 144-pin SODIMMs) available to the ADSP-21160s at 50 MHz
- Site for 1 optional bank (64-512 MB) SDRAM (standard 144-pin SODIMM) available on PCI bus
- 2 banks (one per cluster) 2 MB FLASH RAM available on 8-bit peripheral buses

Link Ports

- 8 link ports extend from the ADSP-21160s (4 per cluster) to rear panel I/O
- 8 link ports (4 per cluster) extend from the ADSP-21160s to the PMC+ sites; optionally cross-connected to the other cluster
- 32 link ports (16 per cluster) dedicated to interprocessor communication

Serial Ports

- 2 serial TDM buses (1 per cluster) extend from the ADSP-21160s to rear panel I/O
- 2 serial TDM buses (1 per cluster) extend from the ADSP-21160s to the PMC+ sites
- 4 RS-232s (one per cluster to rear, one per cluster to front)

PCI Bridges

- 64-bit, 66 MHz single-load interface from PCI backplane to on-board PCI local buses
- Bridge for each cluster to separate cluster and its PMC+ site

SharcFIN ASIC

- 64/66 MHz PCI rev. 2.2 compliant interface (528 burst; 400 MB/s sustained)
- SDRAM controller on SHARC bus; supports up to 512 MB
- SDRAM mapped into PCI memory space
- Programmable interrupt multiplexer: 10 inputs, 7 outputs (supports hardware interrupts in both directions)
- All ADSP-21160 IOP registers and internal SRAM are mapped to PCI memory space
- Supports host- and FLASH-based booting of ADSP-21160 DSPs
- 8-bit, 25 MHz peripheral bus
- Downward compatible with 32-bit, 33 MHz PCI interfaces

PMC+ Interfaces

- Provide connection (via J1–J3) to standard PMC modules
- Provide connection (via J4) to proprietary PMC+ I/O modules for low-latency, high-performance I/O via 4 links and a TDM serial port

Power

- 40W @ 3.3V worst case sustainable
- 2W @ 5V worst case sustainable

Size

- 6U single slot (233mm × 160mm, 9.2"×6.3")

SOFTWARE SUPPORT

Host Interface

- BittWare's software development kit for Windows® 95/98/NT/2000 and Linux contains a C-callable library of board control and communications routines
- Porting kit available for other operating system platforms

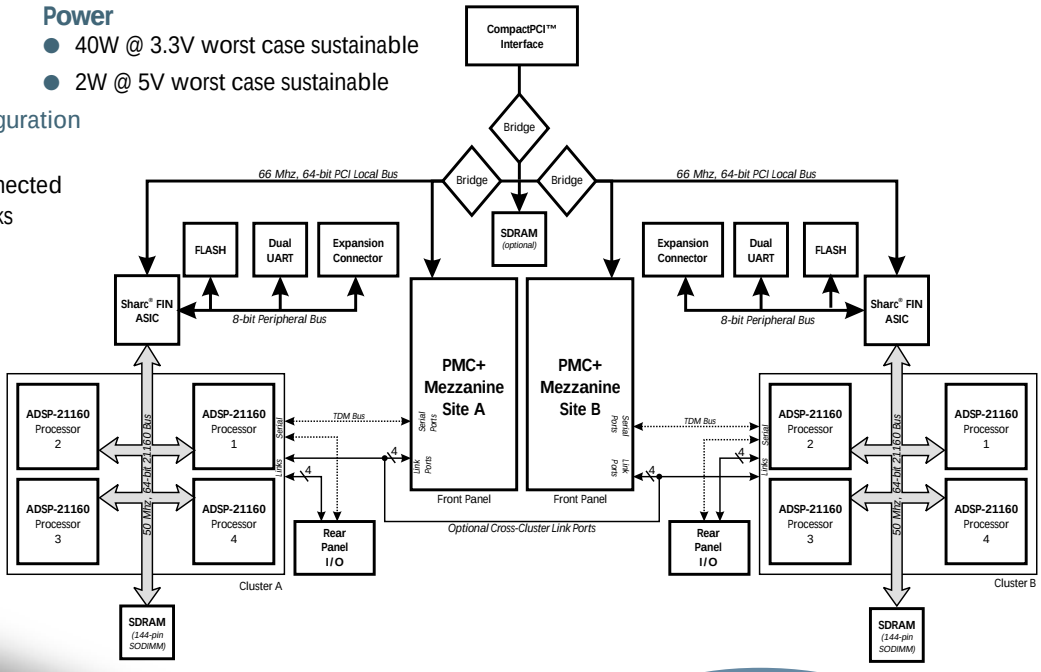
Development Tools

- Analog Devices' VisualDSP tools: C compiler, assembler, linker, simulator, and debugger
- BittWare VisualDSP Target for on-board debugging from host without an ICE
- White Mountain DSP ICE emulators
- Eonic Systems' Virtuoso™ operating system
- BittWare SharcLAB interface to MATLAB Simulink® and Real-Time Workshop®
- BittWare SpeedDSP function libraries

Ordering Information

HH6U-AB-XYZ-AA-L

- **A** — Cluster A Processors
  - 0 DSPs=0
  - 1 DSPs =1
  - 2 DSPs =2
  - 4 DSPs =4
- **B** — Cluster B Processors
  - 0 DSPs=0
  - 1 DSPs =1
  - 2 DSPs =2
  - 4 DSPs =4
- **X** — Shared SDRAM =
  - 64 MB =5
  - 128 MB =6
  - 256 MB =7
  - 512 MB =8
- **Y** — SDRAM A
  - 5= 64 MB
  - 6= 128 MB
  - 7= 256 MB
  - 8= 512 MB
- **Z** — SDRAM B
  - 5= 64 MB
  - 6= 128 MB
  - 7= 256 MB
  - 8= 512 MB
- **AA** — Speed
  - 08= 80 MHz
  - 10= 100 MHz
- **L** — Link Configuration
  - P= PMC+ links
  - X= Cross-connected cluster links



BittWare, Inc.
Tel: 603-226-0404
Fax: 603-226-6667
E-Mail: info@bittware.com

DS-HH6U00-07 (1/01)

SHARC and VisualDSP are registered trademarks of Analog Devices, Inc. All other products are the trademarks or registered trademarks of their respective holders.

BittWare

www.bittware.com