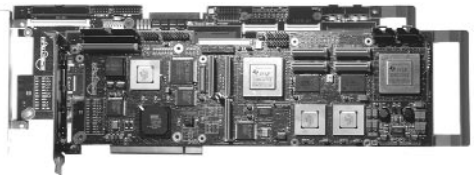
Daytona / Daytona67

Single or Dual 'C6201 or 'C6701 PCI Board



Architecture

Daytona is based on Spectrum's innovative architecture which makes use of Spectrum's revolutionary "Hurricane", a single chip PCI bridge optimized for DSP. This PCI local bus architecture provides:

- data transfer directly in and out of each 'C6x SBSRAM bank from the PMC and host
- data transfer between each processing node's SBSRAM via its Hurricane DMA
- access to each 'C6x DSP's external memory via the host port
- dual ported memory for low latency message passing

Hurricane's internal 64 word FIFO decouples the PCI and DSP bus. This FIFO, combined with Hurricane's DMA engine, allows the host computer read/write access to each node's SBSRAM with minimal interference on the DSP's processing performance.

I/O Methods

Processor Expansion Module (PEM) Sites

PEMs are open specification mezzanine modules that provide 400 MB/s of I/O bandwidth directly into each 'C6x DSP's external bus. A range of Spectrum PEMs are available for I/O, memory, 'C4x Communication Ports and network interfaces.

PMC Site

Hurricane allows the PMC to provide a sustained data rate of 132 MB/s directly into the 'C6x DSP's SBSRAM. Specific PMCs are available to support industry standard interfaces for telecommunications (T1/E1), networking, bus interface, mass storage, and intelligent I/O processing.

DSP~LINK3™

DSP~LINK3™ is a deterministic memory-mapped interface that provides up to 30 MB/s of I/O bandwidth. DSP~LINK3™ is an open specification which interfaces to the Daytona I/O mezzanine site, to IndustryPack® I/O, and to custom I/O. Daytona can interface to over 150 different IndustryPack® I/O modules available from a variety of vendors.

Software

Host OS - WindowsNT®.

Host Compilers - Microsoft's Visual C++® and Visual Basic®.

Host Interface Library and Driver - provides a standard product and OS independent set of C functions for Host-DSP communications including DSP code download, data transfer and interrupts.

DSP Application Tools - MathWorks' Matlab® and Hyperception's Hypersignal® Software Products.

Daytona Board Support DSP Library - provides a standard product independent set of C functions that encapsulate complex board level tasks like PCI bus mastering and PCI interrupt generation.

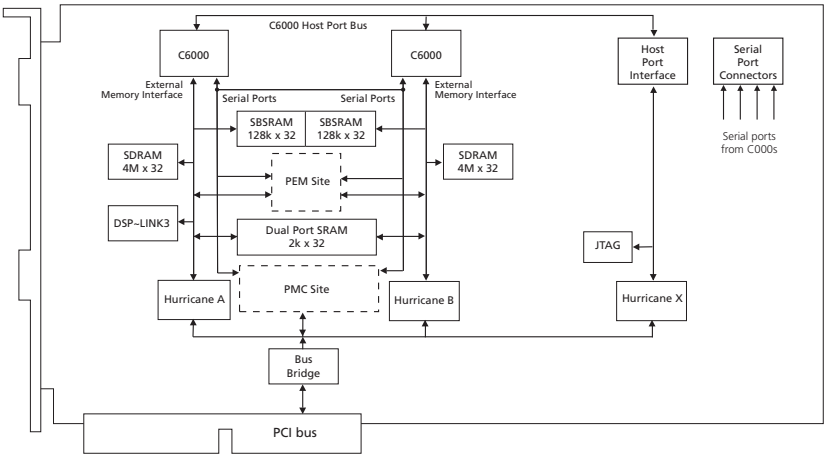
TI Code Generation Tools - 'C6201 or 'C6701 C/Assembler/Optimizer.

DSP Debugging - Texas Instruments' Code Composer Studio™ operates across the VME bus, therefore external emulation hardware is not required.

DSP RTOS - Diamond is an advanced, yet simple to use, DSP RTOS that schedules multiple tasks across multi-DSP systems. Diamond allows for easy hardware reconfiguration and migration.

Signal Processing Libraries - various general purpose (FFT, filtering) and application-specific libraries are available. Source code for DSP software libraries is provided.

- **Processor Choice:**
  - **Single or Dual 1600 MIPS, 200 MHz TMS320C6201B DSPs**
  - **Single or Dual 1 GFLOPS, 167 MHz TMS320C6701 DSPs**
- **Innovative board architecture eliminates data double handling**
- **Comprehensive software support:**
  - **Host Interface Library and Drivers**
  - **Daytona board support DSP Library**
  - **Code Composer Studio™**
  - **Diamond, a multi-DSP RTOS**
- **1 MB of SBSRAM (max) and 32 MB of SDRAM (max)**
- **8K x 32 dual port memory for low latency and deterministic inter-processor communication**
- **SBSRAM distributed shared memory**
- **Hurricane, a single chip PCI bridge optimized for DSP systems**
- **Flexible I/O interfaces:**
  - **One PEM site provides 400 MB/s per DSP**
  - **One PMC provides 132 MB/s throughput**
  - **DSP~LINK3™ provides up to 30 MB/s for interfacing to an Analog I/O mezzanine site and other open I/O solutions**
- **IndustryPack® (IP) support for over 150 different industry standard I/O modules**
- **'C6000 technical training workshops available**



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PCI

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