Daytona
Dual 'C6x PCI Board
Technical Reference

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Preface

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- EN50082-1 Electromagnetic Immunity

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Board products with the CE marking have been tested in a representative system to show compliance with the preceding requirements. A proper installation in a CE-marked system shall maintain the required EMC/safety performance.

Document Change History

Rev.	Date	Changes	Section
2.01	Feb 2000	Updated document format	n.a.
		Corrected IRBAR register address and value	2.4
		Corrected ‘C6x memory map	3.1
		Added note about 32-bit Dual-Port RAM accesses	3.10
		Moved CE Mark info from section 11 to Preface	11

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1 Introduction

This manual describes the features, architecture, and specifications of the Daytona Dual 'C6x PCI Board. It will help you understand how the function libraries described in the *Daytona Programming Guide* operate within the board. You can also use this information to program the board at a driver level, extend the standard hardware functionality, or obtain more information to do custom configurations.

1.1. Features

Spectrum's Daytona full-width PCI board consists of two TMS320C6x processing nodes, and is available with TMS320C6x processors for either fixed-point or floating-point operation.

Product	Operation	Processors	Processor Clock Speed
Daytona	Fixed-point	TMS320C6201 (Revision B)	200 MHz
Daytona67	Floating-point	TMS320C6701	167 MHz

Both the Daytona and the Daytona67 are referred to as "Daytona" in this manual unless otherwise noted.

Daytona has the following features:

- Up to two TMS320C6201 or TMS320C6701 processing nodes
- 128K x 32-bit of Synchronous SRAM per processing node
- 4M x 32-bit of SDRAM per processing node
- 8K x 32-bit of dual-port RAM supporting low-latency data exchange between processing nodes
- Host PCI interface using the DEC21153 PCI-to-PCI bridge chip
- 132 MBytes/s PMC module site
- Convenient paged memory access to the 'C6x address space through the 'C6x Host Port Interface (HPI)
- External and on-board JTAG debugging support
- PEM (Processor Expansion Module) sites
- DSP~LINK3 I/O interface

1.1.1. PCI Interface

A local PCI bus on the Daytona connects the processor nodes, system control operations, and the PMC site together. The DEC 21153 chip provides the PCI-to-PCI bridge from this local PCI bus to the external host PCI bus.

Spectrum's Hurricane chip provides a high performance bridge between the PCI bus and DSP processors. Each processing node is connected to the local PCI bus through a Hurricane chip. A Hurricane chip is also used as the interface between the 'C6x Host Port Interface bus and test bus controller system control operations, and the local PCI bus.

1.1.2. PMC Interface

A PMC site is provided on the board that is accessible from both the local PCI bus and host PCI bus. The PMC site allows a PMC (PCI Mezzanine Connector) card to be installed in order to add I/O, memory, or other capabilities to the Daytona.

1.1.3. PEM Module Site

One PEM (Processor Expansion Module) site is provided that supports a single-width PEM. The PEM site provides a pair of high-speed bi-directional 'C6x processor interfaces. They are available for computer telephony, digital radio as well as customer-specific interfaces.

1.1.4. DSP~LINK3 Interface

A DSP~LINK3 interface is provided for both on-board and external I/O boards (such as IndustryPack boards). The DSP~LINK3 interface is controlled via processing node A.

1.1.5. Serial Ports

The two serial ports of each 'C6x can be routed to the PEM site, the PMC connector, or between the processors under host software control. Serial port 0 from each process can also be routed to external connectors on the Daytona.

1.1.6. JTAG Debugging Support

A PCI host can access an on-board JTAG Test Bus Controller (TBC) from the PCI Bus for diagnostic purposes. JTAG connectors are also provided for external JTAG debugging.

1.2. Reference Documents

Daytona Installation Guide available from Spectrum

Daytona Programming Guide available from Spectrum

Hurricane Data Sheet available from Spectrum

DSP~LINK3 Specification available from Spectrum

PEM Specification available from Spectrum

TMS320C6201/C6701 Peripherals Reference Guide available from Texas Instruments

Digital Semiconductor 21153 PCI-to-PCI Bridge Data Sheet available from Intel

PCI Local Bus Specification Rev. 2.1 available from PCI Special Interest Group

IEEE P1386/Draft 2.0 (April 4, 1995) Common Mezzanine Card Family

IEEE P1386.1/Draft 2.0 (April 4, 1995) Physical and Environmental Layers for PCI Mezzanine Cards

1.3. Bus Architecture

A block diagram of the Daytona is shown in the following figure.

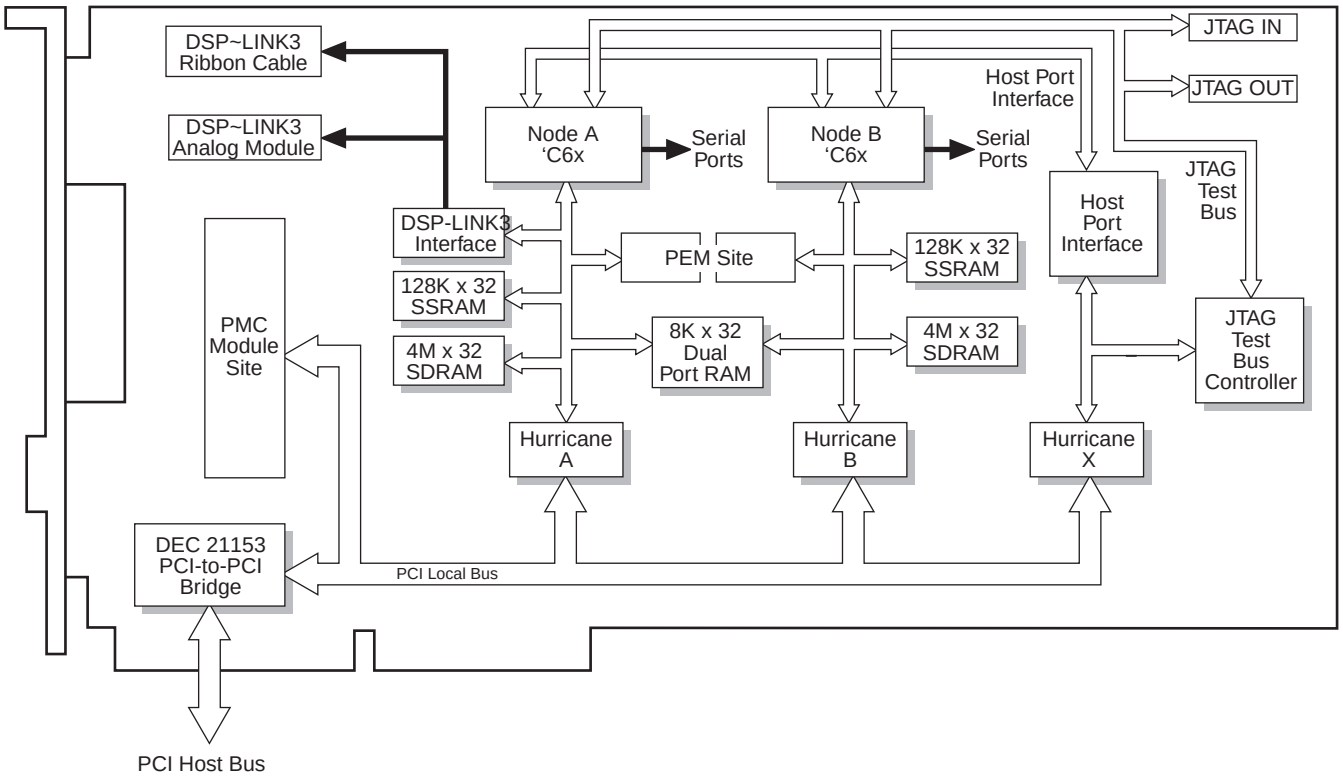


Figure 1 Block Diagram

1.4. Reset Information

The following table shows which Daytona components and interfaces are reset by the different reset conditions that can be initiated.

Table 1 Component and Interface Reset Conditions

Component/Interface	PCI Bus RST#	Hurricane X Reset Register	Daytona Reset	JTAG Reset	DSP~LINK3 Reset
DEC 21153	**Y**				
PMC Site	**Y**				
Hurricane X	**Y**				
Hurricane A	**Y**				
Hurricane B	**Y**				
System Control Logic	**Y**	**Y**			
Processor Node Logic	**Y**	**Y**	**Y**		
PEM Site	**Y**	**Y**	**Y**		
JTAG*	**Y**	**Y**	**Y**	**Y**	
DSP~LINK3	**Y**	**Y**	**Y**		**Y**

*These functions reset on-board emulators and switching logic. External emulators must be reset separately.

Reset Condition	Description
PCI Bus RST#	Asserting the RST# pin on the host PCI bus resets the entire Daytona board.
Hurricane X Reset	Any PCI device can generate this reset by writing a '1' to the ASSERT RESET bit (D16) of the Hurricane X **Register Access and Status Control Register (RAC)**. This register can be accessed at address offset 0x0004 003C within the Hurricane X memory space. To release reset, write a '1' to the NEGATE RESET bit (D17) of this register after a minimum delay of 10 ms.
Daytona Reset	Any PCI device can generate this reset by writing a '1' to the RESET bit (D0) of the Daytona **Reset Register**. This register can be accessed by a PCI device at the Hurricane X Base Address 0 offset 0x0008 0000.
JTAG Reset	Any PCI device can generate this reset by writing a '1' to the JTRST bit (D2) of the Daytona **Reset Register**. This register can be accessed by a PCI device at the Hurricane X Base Address 0 offset 0x0008 0000.
DSP~LINK3 Reset	Applications running on the node A 'C6x can reset the DSP~LINK3 interface by writing a '1' to the DL3_RST bit (D4) of the **DSP~LINK3 Control Register**. This register can be accessed at the node A 'C6x address 0x0170 001C.

1.5. Board Layout

The following board layout diagrams show the locations of the various components, connectors, DIP switches, and LEDs on Daytona.

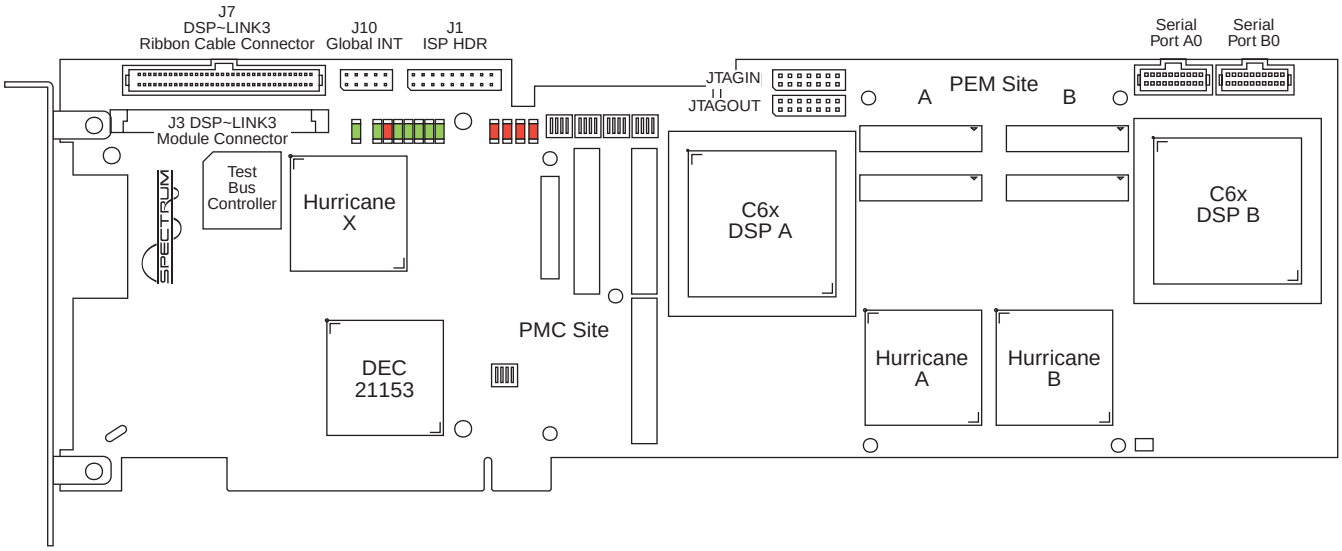


Figure 2 Connector and Component Locations

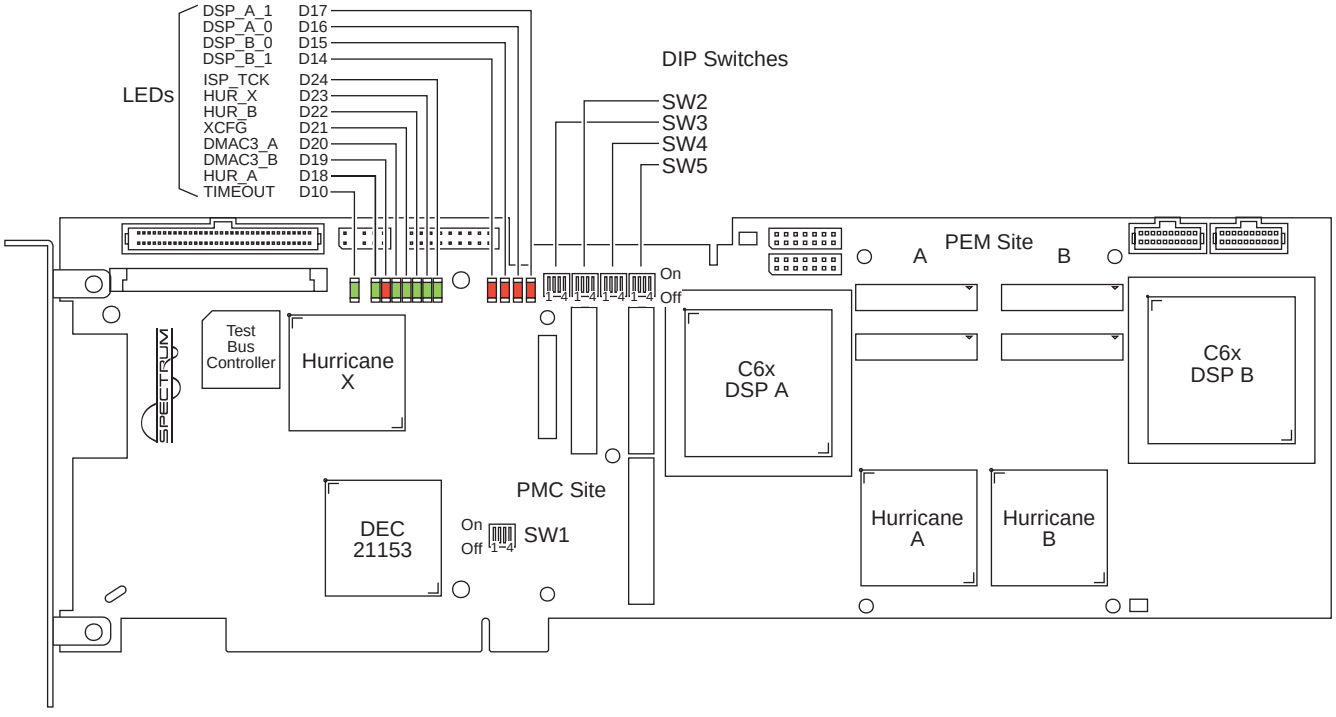


Figure 3 DIP Switch and LED Locations

1.6. DIP Switch Settings

There are five 4-position DIP switches on the Daytona board. SW1 is located above the PCI card edge connector and is covered if a PMC module is installed. SW2 to SW5, located at the top of the board, are accessible even if a PMC or DSP~LINK3 module is installed on the Daytona.

Table 2 DIP Switch Settings

DIP Switch	Position	On	Off	Description
SW1	1	*Reserved	Reserved	Must be ON (factory use only)
	2	*Reserved	Reserved	Must be ON (factory use only)
	3	*Reserved	Reserved	Must be ON (factory use only)
	4	Reserved	*Reserved	Must be OFF (factory use only)
SW2	1	*0	1	Board ID – bit 3
	2	*0	1	Board ID – bit 2
	3	*0	1	Board ID – bit 1
	4	*0	1	Board ID – bit 0
SW3	1	ROM	*HPI	DSP Boot Source
	2	Disabled	*Enabled	Route PMC INTB#, INTC#, and INTD# to PCI bus
	3	Disabled	*Enabled	Route PMC INTA# to PCI bus
	4	Internal	*EEPROM	Hurricane Configuration (Must be OFF)
SW4	1	Reserved	*Reserved	Must be OFF (for future use)
	2	*Reserved	Reserved	Must be ON (for future use)
	3	Reserved	*Reserved	Must be OFF (for future use)
	4	*Reserved	Reserved	Must be ON (for future use)
SW5	1	Reserved	*Reserved	Must be OFF (for future use)
	2	*Reserved	Reserved	Must be ON (for future use)
	3	Reserved	*Reserved	Must be OFF (for future use)
	4	*Reserved	Reserved	Must be ON (for future use)

*Factory default setting

1.7. Status LEDs

The following table describes the LEDs on the Daytona.

Table 3 LED Descriptions

LED	Label	Description
D10	TIMEOUT	Indicates if an HPI timeout error condition is inhibiting HPI operation. ON if there is a HPI timeout error
D18	HUR_A	State of the GPIO2 pin of Hurricane A. ON when GPIO2 is low.
D19	DMAC3_B	State of the DMAC3 pin of the Node B ‘C6x. ON when DMAC3 is low.
D20	DMAC3_A	State of the DMAC3 pin of the Node A ‘C6x. ON when DMAC3 is low.
D21	XCFG	Configuration state of the board’s FPGA devices. ON during system reset. OFF during normal operation.
D22	HUR_B	State of the GPIO2 pin of Hurricane B. ON when GPIO2 is low.
D23	HUR_X	State of the GPIO2 pin of Hurricane X. ON when GPIO2 is low.
D24	ISP_TCK	Factory use only
D14	DSP_B_1	User defined via bit 1 in the **LED register** of node B
D15	DSP_B_0	User defined via bit 0 in the **LED register** of node B
D16	DSP_A_0	User defined via bit 0 in the **LED register** of node A
D17	DSP_A_1	User defined via bit 1 in the **LED register** of node A

1.7.1. ‘C6x DMAC3 LEDs

The state of the DMAC3 LED of each ‘C6x is user-defined through the DMA channel 3 Secondary Control Register (0x0184 004C) of the DSP. Bits [18:16] of this register should be 000 to turn LED on and 001 to turn it off. Refer to *TMS320C6201 Peripheral Guide* for further information.

1.7.2. Hurricane GPIO2 LEDs

The output of the General Purpose I/O 2 pin (GPIO2) of each Hurricane is indicated by an LED. These pins are controlled through bits 8, 9, 14, and 15 of the Hurricane's **General Control and Status Register** (GCSR) at address offset 0x014 from the beginning of the Hurricane register space.

- Write 0x0000 8200 to turn the LED on.
- Write 0x0000 8100 to turn the LED off.

These LEDs are ON upon reset.

1.7.3. Diagnostic LEDs

Two LEDs can be used for hardware diagnostic purposes: the TIMEOUT LED (D10) and the XCFG LED (D21).

- The TIMEOUT LED indicates that an HPI timeout condition has occurred. Refer to the section describing HPI timeouts in this manual for more information.
- The XCFG LED is lit while the PCI system reset is active, and goes off when PCI reset is deasserted. If it remains lit, the board will not function; SW1 is incorrectly set, there is a system problem, or there is a hardware failure.

All other LEDs are modified by software and can be used for application development diagnostics.

2 PCI Bus Interface

The Daytona is fully PCI revision 2.1 compliant through its card edge connector for +5 Volt operation. The DEC 21153 provides a PCI-to-PCI bridge between the Host PCI bus and a PCI local bus on the board. The PCI local bus connects DEC 21153 to the Hurricane chips of the processors and to Hurricane X. Any device on the local PCI bus is accessible, through the DEC 21153, to the host PCI bus.

2.1. DEC 21153 Host PCI Interface

The DEC 21153 provides the interface between the host PCI bus and the local PCI bus on the Daytona. Resources, such as the PMC site and Hurricane chips are assigned PCI device numbers. The following table shows the PCI device number assignments; all other devices numbers are reserved.

Table 4 PCI Device Number Assignment

Device Number	Resource	Description
0	PMC site	PCI Mezzanine Connector site
2	Hurricane X	PCI-to-DSP bridge to the HPI bus, test bus controller, and general system registers.
3	Hurricane A	PCI-to-DSP bridge to processor node A SSRAM
4	Hurricane B	PCI-to-DSP bridge to processor node B SSRAM

The system BIOS or operating system configure the base address and limit registers for memory and I/O transactions in order to determine which transaction cycles are forwarded from the host PCI bus to the Daytona local PCI bus. Memory and I/O cycles falling outside the bounds set by these registers are not forwarded.

Type 1 Configuration cycles from the host PCI to the DEC 21153 are forwarded to the local PCI bus, while type 0 Configuration cycles are used to configure the DEC 21153.

2.2. General PCI Memory Map

The Hurricane chips and PMC site on the Daytona act as PCI devices. As such, they each present a memory map to the PCI bus. The memory map of an installed PMC module depends upon the module, but the maps of the processor node Hurricane chips and Hurricane X are determined by the board. The DEC 21153 PCI-to-PCI bridge chip is configured with the base address each of these maps by the BIOS at PCI reset. Each device has a base address 0 (BAR0) which marks the beginning of its memory map.

The PCI devices of the Daytona board are mapped within the PCI bus as shown in the following diagram.

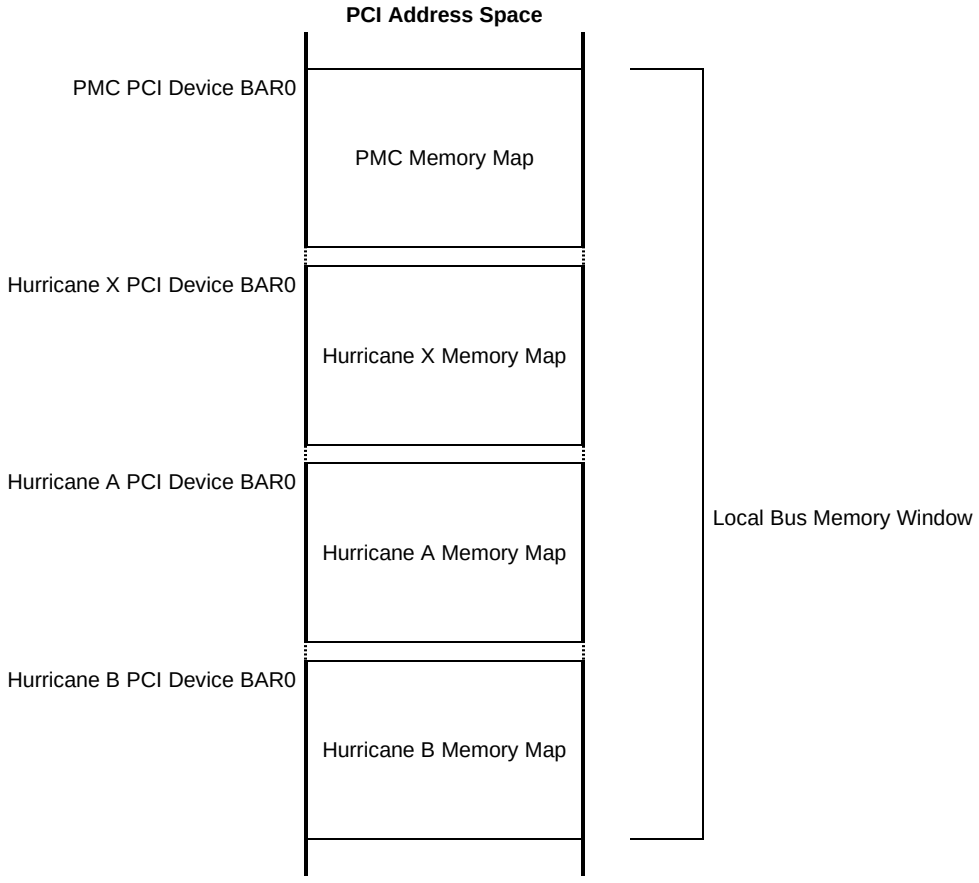


Figure 4 General PCI Memory Map

2.3. Local PCI Bus Arbitration

The DEC 21153 supports a prioritized arbitration mechanism for the local PCI bus. Any PCI device that transfers data across the local PCI bus can be assigned either to a high priority group or a low priority group.

The entire low-priority *group* has a priority weight equal to a single high priority *device*. Access priority will rotate evenly around all high-priority devices and then to the low

priority group as a whole. Each time the priority rotates to the low priority group, priority will be assigned to a new device within that group.

If a high priority device requests the bus while a low priority master is transferring data, the low priority transfer will be halted, and the bus granted to the high priority device. Priorities are reevaluated at the start of each new transaction on the local PCI bus.

Upon reset, external PCI bus masters have high priority, and all local devices have low priority. An external bus master is any PCI device on the other (host) side of the DEC bridge. The local devices on the Daytona are:

- PMC site
- Hurricane X
- Hurricane A
- Hurricane B

These priorities can be customized by using the **Arbiter Control Register** of the DEC 21153. This register is a device-specific configuration register occupying the upper 16 bits [31:16] of address offset 0x42 within the DEC 21153 PCI configuration space. The arbitration of the Daytona local PCI bus can therefore be changed by setting this register. Refer to the *Digital Semiconductor 21153 PCI-to-PCI Bridge Data Sheet* from Intel for complete information on how this register affects bus arbitration.

Each bus master is assigned to a low or high priority group by setting the corresponding bit in the **Arbiter Control Register**. These bits are shown in the following figure along with the default reset values, and a set of values for a subsequent example. If the bit is set to 1, the master is assigned to the high priority group. If the bit is set to 0, the master is assigned to the low priority group. As can be seen, only external bus masters are assigned a high priority upon reset (default); all other devices are low priority.

External bus masters represent any PCI master on the other side of the DEC 21153 bridge, such as the PCI host computer in which the Daytona board is installed.

	D31.. ..D26	D25	D24
	Reserved	External Bus Masters	Reserved
Default	*set to 0's*	*1*	*0*
Example	*set to 0's*	*1*	*0*

	D23	D22	D21	D20	D19	D18	D17	D16
	Reserved	Reserved	Reserved	Hurricane B	Hurricane A	Hurricane X	Reserved	PMC Site
Default	*0*	*0*	*0*	*0*	*0*	*0*	*0*	***0***
Example	*0*	*0*	*0*	*0*	*0*	*0*	*0*	***1***

Figure 5 DEC21153 Arbiter Control Register

The following lists show sample arbitration sequences for both the default and example values given in the preceding register. In the default values only external bus masters are

given high priority. In the example values, external bus masters and the PMC site are both given high priority by changing bit D16 to a '1'. (High priority bus masters are shown in **bold**; low priority bus masters are shown in *italics*.)

Default Value Arbitration Sequence	Example Value Arbitration Sequence
1. **External Bus Master**	1. **PMC Site**
2. *PMC Site*	2. **External Bus Master**
3. **External Bus Master**	3. *Hurricane X*
4. *Hurricane X*	4. **PMC Site**
5. **External Bus Master**	5. **External Bus Master**
6. *Hurricane A*	6. *Hurricane A*
7. **External Bus Master**	7. **PMC Site**
8. *Hurricane B*	8. **External Bus Master**
9. **External Bus Master**	9. *Hurricane B*
10. *PMC Site*	10. **PMC Site**
and so on…	11. **External Bus Master**
	12. *Hurricane X*
	and so on…

2.4. Hurricane X Memory Map

The PCI memory map of Hurricane X supports several system control functions for the Daytona board. These are shown in the following Hurricane X memory map.

Note: PCI address offsets are given from the BAR0 base address of the Hurricane. The memory map is byte-addressed (1 byte of data per location), but is aligned along 32-bit word boundaries to accommodate the 32-bit data words.

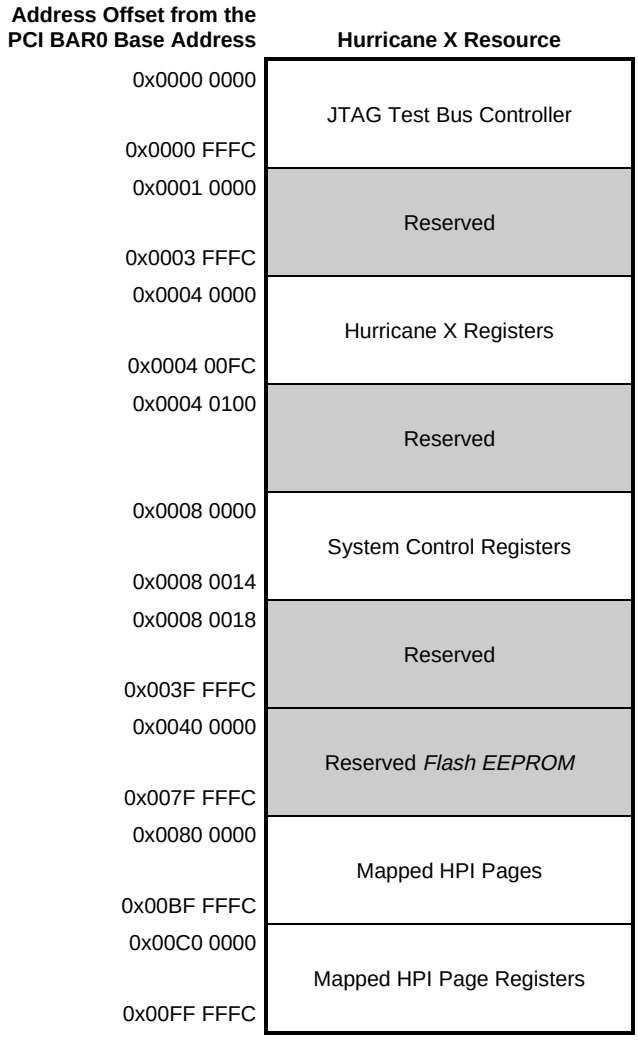


Figure 6 Hurricane X Memory Map

After reset the Hurricane X register set is not visible until the Hurricane's IRBAR (**I**nternal **R**egister **B**ase **A**ddress **R**egister) has been configured to define the PCI base address for the internal registers. The value written to the IRBAR register is determined by adding 0x0004 0000 to the PCI base address of Hurricane X. The Hurricane's PCI base address can be found by reading the BAR0 configuration register of Hurricane X. Even though the Hurricane register set is not visible, the host can write to the IRBAR register at address BAR0 + 0x0004 00EC.

Note: The software drivers supplied with Daytona automatically perform the correct IRBAR configuration.

2.5. Mapped HPI Pages

The addressable memory space seen by each processor can be accessed from the local PCI bus through a set of 8 mapped 64 KB windows. A device on the PCI bus accesses these memory pages through the Mapped HPI Pages space of the Hurricane X memory map. The Mapped HPI Pages space uses the ‘C6x Host Port Interface (HPI) to provide a set of 64 KB windows into the memory space of each processor.

Each of a node’s eight memory pages has a corresponding set of registers for configuring the location and operation of the page.

Note: The Mapped HPI Page feature is enabled by the MAPON bit of the Daytona **Configuration Register** accessed through the PCI local bus at offset 0x0008 0004 from the Hurricane X BAR0 address.

2.5.1. Mapped HPI Pages Memory Map

The following figure shows how the memory pages are organized in the Mapped HPI Pages space. Addresses are given as byte offsets from the PCI base address (BAR0) of Hurricane X.

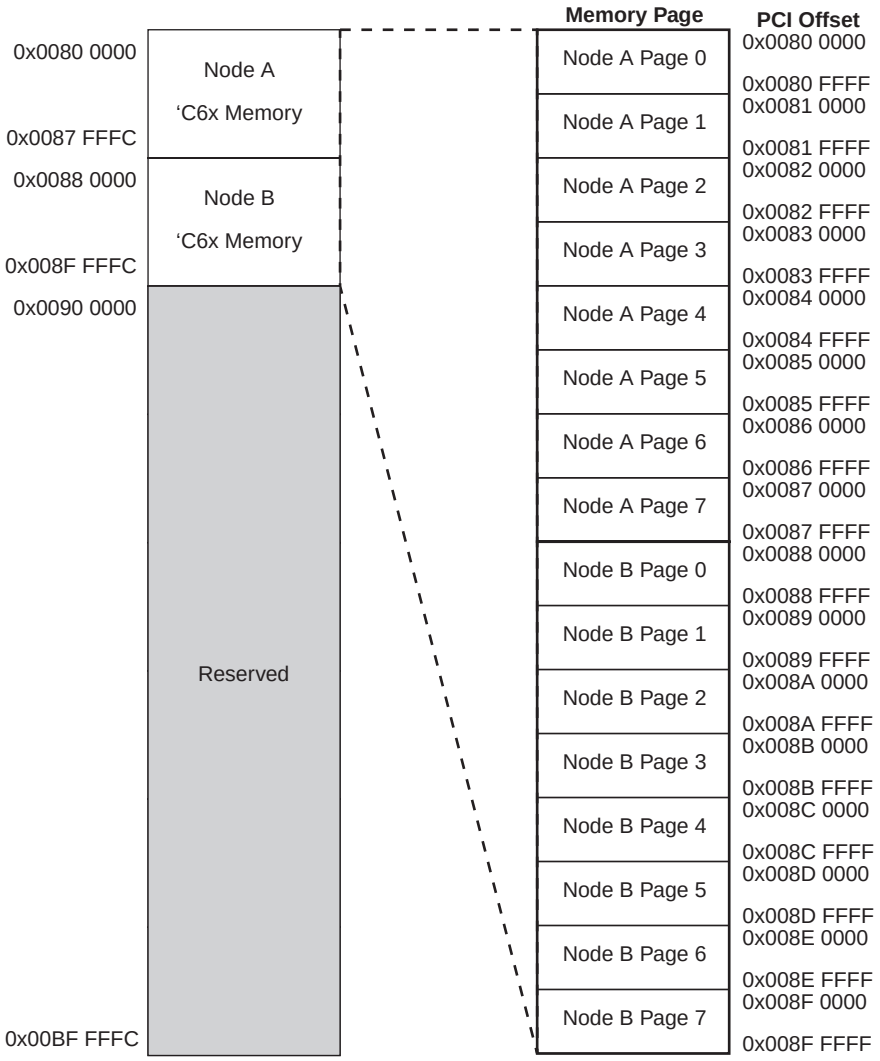


Figure 7 Mapped HPI Pages Memory Map

2.5.2. Mapped HPI Page Registers

Location and operation of each memory page is configured through registers in the *Mapped HPI Page Registers* region of the Hurricane X memory map. Within this address region, each memory page has a corresponding set of registers. The following figure shows how these register sets are organized within the HPI Register region.

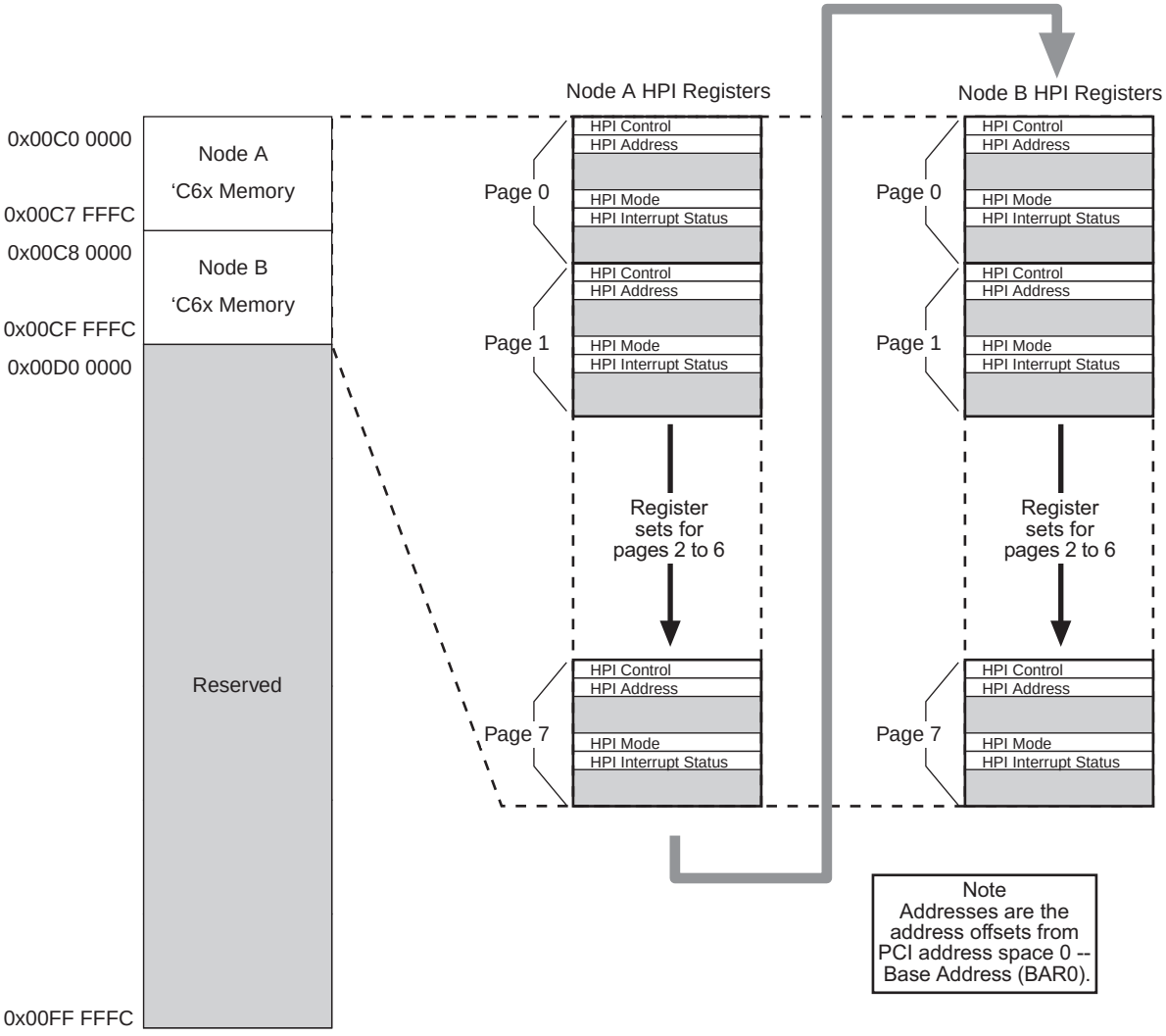


Figure 8 Mapped HPI Page Registers

The register set for each memory page consists of four registers. These registers are similar to the HPI registers within the ‘C6x processor. Complete definitions and addresses of these registers is given in section 9, *PCI Addressable Registers*.

HPI Control Register Controls and monitors the operation of HPI for mapped memory pages. Its functions include:

- Generating interrupts to the ‘C6x for the memory page through the register’s DSPINT bit (D1). Each memory page has its own interrupt flag. The processor node’s **HPI Interrupt** register indicates whether the interrupt flag for a particular memory page has been set.
- Monitoring and clearing the HINT interrupt generated from the DSP to the PCI host through the register’s HINT bit (D2).

HPI Address Register Used to set the base address within the ‘C6x memory for the memory page.

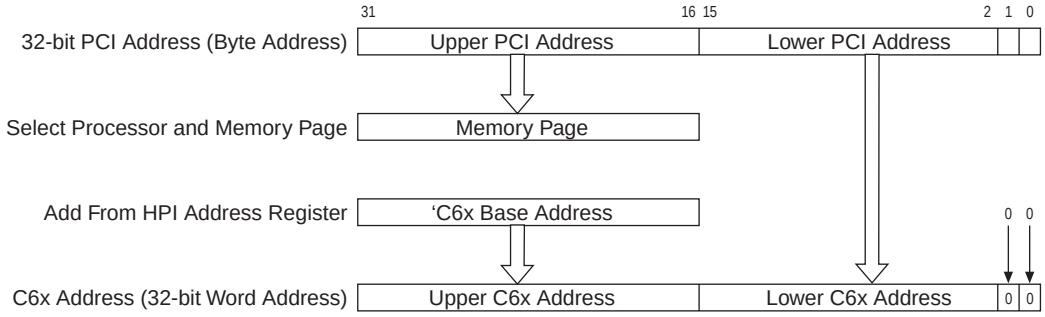
HPI Mode Register Reserved for future compatibility.

HPI Interrupt Status Indicates the state of the interrupt flag that is set when an interrupt is generated by the memory page’s **HPI Control Register**. Each memory page has its own interrupt flag.

2.5.3. Mapped HPI Pages Address Translation

The base address for each 64K memory page is set by the **HPI Address register** for that page. The upper 16 bits of the base address, which must be aligned to a 64K byte address boundary, is placed in the upper 16 bits of the **HPI Address register**. When a device on the PCI bus addresses a location within the memory page, the actual address to the ‘C6x location is determined from this value in the register and the lower 16 bits of the address on the PCI bus. Because the HPI port is word (32-bit) addressed, the lower 2 bits (D[1..0]) of the PCI address are set to ‘0’ when added to the ‘C6x base address.

The following figure shows this address translation.



2.5.4. Using Mapped HPI Pages

The mapped HPI memory pages provide a convenient way to access the ‘C6x memory space from the PCI bus. The following steps configure the Daytona to use mapped HPI pages.

1. Set the HWOB bit by writing ‘0x0001 00001’ to the **HPI Control Register**. This register is accessible from the PCI bus at address offset 0x00C0 0000 from PCI base address 0 (BAR0) of Hurricane X.

2. Enable the HPI address translation for the board by setting the MAPON bit (D0) of the **Configuration Register** to ‘1’. This register is accessed from the PCI bus at address offset 0x0008 0004 from PCI base address 0 (BAR0) of Hurricane X.

3. Set a base address in the **HPI Address Register** for each memory page. Each DSP has eight of these registers corresponding to the eight memory pages. Refer to *Table 13 Mapped HPI Page Register Addresses* for the register address offsets from PCI address space 0.

The memory space of the ‘C6x processors can now be accessed from the PCI bus through the configured memory pages.

Note: The FETCH bit of the **HPI Control Register** and the PREF bit of the **HPI Mode Register** do not have to be set for enhanced HPI processor access. They should be left alone.

2.5.5. Mapped HPI Pages Interrupt-Driven Signaling

A PCI host can use interrupt-driven signaling to notify a DSP of memory page accesses. This is provided through the HPI interrupt of the ‘C6x.

1. A PCI host generates an HPI interrupt to the ‘C6x by setting the DSPINT bit of the **HPI Control register** of a particular memory page to ‘1’.

2. Upon receiving the interrupt, the ‘C6x reads the **HPI Interrupt register** to determine which page, if any, generated the interrupt.

3. The ‘C6x can then clear the interrupt through the **HPI Interrupt register** as well.

A PCI host can read the state of the DSPINT bit of the **HPI Control register** of any page to determine if any page has generated an HPI interrupt to the ‘C6x which has not been cleared.

To determine if a particular page has generated an HPI interrupt to the ‘C6x which has not been cleared, the host can read the ISTAT bit (bit D1) of the **HPI Interrupt Status register** for the particular memory page.

Complete information on these registers can be found in sections 9 and 10.

2.6. HPI Time-outs

The Daytona board provides an HPI time-out mechanism to prevent unrecoverable bus errors resulting from deadlocked Hurricane cycles to the HPI. A ‘C6x crash or software error may result in this condition. While the problem that created the error condition is not resolved, the system software is able to fail gracefully, without a total system failure or shutdown.

For deadlocked cycles caused by hardware or software problems, the PCI specification allows PCI devices to abort transfers and shut down offending devices. Error control in this event is typically dependent upon the system’s BIOS and design. In some Windows NT systems, such as a computer with an older BIOS, a total and unrecoverable system crash can occur.

The Daytona time-out mechanism avoids this by monitoring the length of an HPI access cycle. If the cycle does not complete within a set time, the following actions are taken.

1. The controller aborts the cycle and returns READY to Hurricane X.
2. The Time-out bit (D8) of the **Reset Register** is set to ‘1’.
3. The TIMEOUT LED is lit.
4. Further accesses to the host port are inhibited.
5. Subsequent PCI bus cycles are completed, but no data is transferred.

To resume HPI accesses, the **Reset Register** Time-out bit must be cleared by writing a ‘1’ to it. The **Reset Register** can be accessed through Hurricane X from the PCI bus at offset 0x0008 0000 from PCI base address 0 (BAR0) of Hurricane X.

2.7. Basic HPI Access

Although the mapped HPI memory pages can provide the best access to the 'C6x memory space from the PCI bus, basic HPI access to the Daytona 'C6x processors is also supported. Refer to the *Host-Port Interface* section of the *TMS320C6201/ C6701 Peripherals Reference Guide.* The interface consists of the following 32-bit registers.

- HPI Address register (HPIA)
- HPI Control register (HPIC)
- HPI Data registers (HPID)

Basic HPI access is selected by setting the MAPON bit (D0) of the **Configuration Register** to '0'. This register is accessed by a master on the local PCI bus at address offset 0x0008 0004 from PCI base address 0 (BAR0) of Hurricane X.

The base addresses for the HPI registers – when MAPON is set to '0' – are given in the following table.

Table 5 HPI Register Addresses

'C6x Register	Node A Address Offset	Node B Address Offset	Description
HPIC	0x00C0 0000	0x00C8 0000	Sets the state for reading and setting the Control Register value.
HPIA	0x00C0 0004	0x00C8 0004	Used to read and set the HPI address pointer. The HPIA points into the 'C6x memory space.
HPID	0x00C0 0008	0x00C8 0008	*Reserved. Do **not** use this register.*
HPID	0x00C0 000C	0x00C8 000C	A PCI host reads and writes data to this address for single cycle transfers to the HPID register. The HPIA is not incremented for this HPI access mode.

Important! Bits D[31..16] of the HPIC register *must* be programmed with the same values programmed into bits D[15..0], and the HWOB bit must *always* be set to '1' whenever writing to the HPIC register. For example, to set the HWOB bit, write 0x00010001 to this register. Refer to the *TMS320C6201/ C6701 Peripherals Reference Guide* for complete information about the HPI Control Register (HPIC).

To access an address within a 'C6x's memory space, the PCI device loads the address into the HPIA register. Data is then transferred through the HPID register.

2.8. Processor Node Hurricane Memory Map

Any master on the local PCI bus has read/write access to the SSRAM of each node through the node's Hurricane chip. The SSRAM is mapped to two regions of the PCI bus: a standard read/write region and a fast write-only region. The **SSI Interrupt Register** is also provided which allows a PCI host to interrupt the node's 'C6x processor. The processor nodes present identical memory maps to the PCI local bus, but are seen as different devices on the PCI local bus.

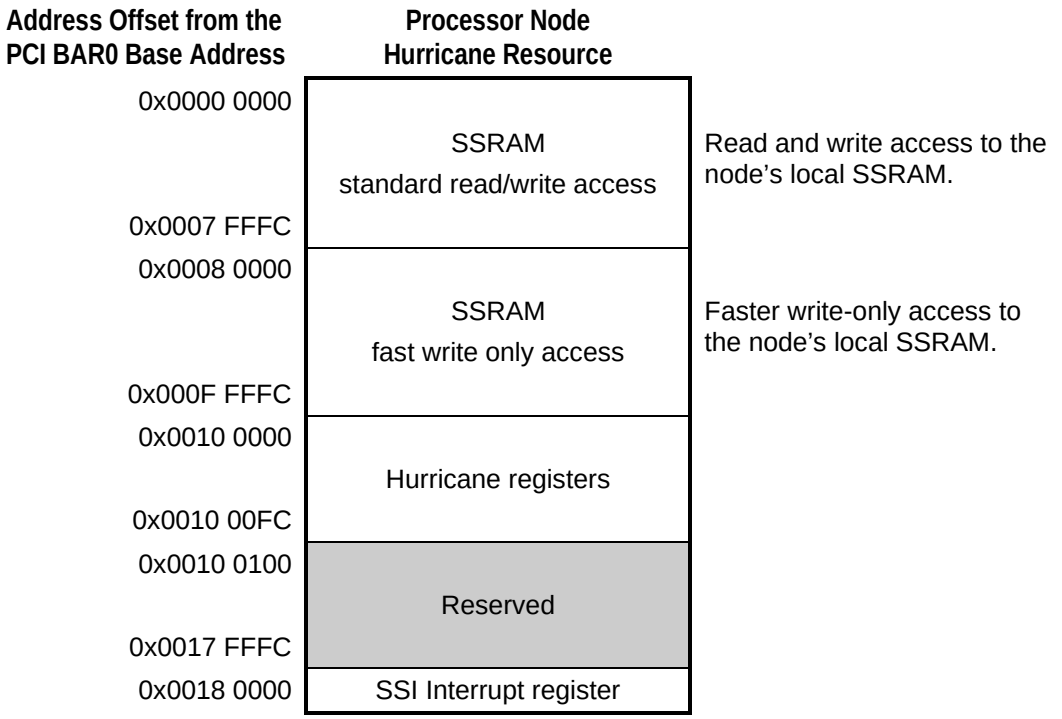


Figure 9 Processor Node Hurricane Memory Map

Note: Hurricane A and Hurricane B resources can be accessed from the PCI bus only after their DSPs have been booted, and external bus requests have been enabled. If any device attempts to access these resources before this time, a system crash may result.

After reset the Hurricane register set is not visible until the Hurricane's IRBAR (**I**nternal **R**egister **B**ase **A**ddress **R**egister) has been configured to define the PCI base address for the internal registers. The value written to the IRBAR register is determined by adding 0x0010 0000 to the PCI base address of the Hurricane. The Hurricane's PCI base address can be found by reading the BAR0 configuration register of the Hurricane.

Although the Hurricane register set is not visible, the IRBAR register can be written to by both the host (BAR0 + 0x0010 00EC) and by the DSP (0x0178 00EC). The library calls in the Daytona Software Development Kit (SDK) set this register from the DSP, which is the easiest method. This register can be set by the host only after the DSP has booted, and after it has enabled external bus requests.

3 Processor Nodes

The Daytona supports two TMS320C6x DSP nodes. The nodes have identical sets of resources, except that node A also supports the board's DSP~LINK3 interface:

- One TMS32C6201 fixed-point DSP for Daytona, or one TMX230C6701 floating-point DSP for Daytona67
- 512 KB (128K x 32) Synchronous SRAM (SSRAM)
- 16 MB (4M x 32) Synchronous DRAM (SDRAM)
- 32 KB (8K x 32) dual-port RAM shared with both nodes
- Processor Expansion Module (PEM) interface
- Host Port Interface to the PCI bus via a Hurricane chip
- DSP~LINK3 interface (processor node A only)

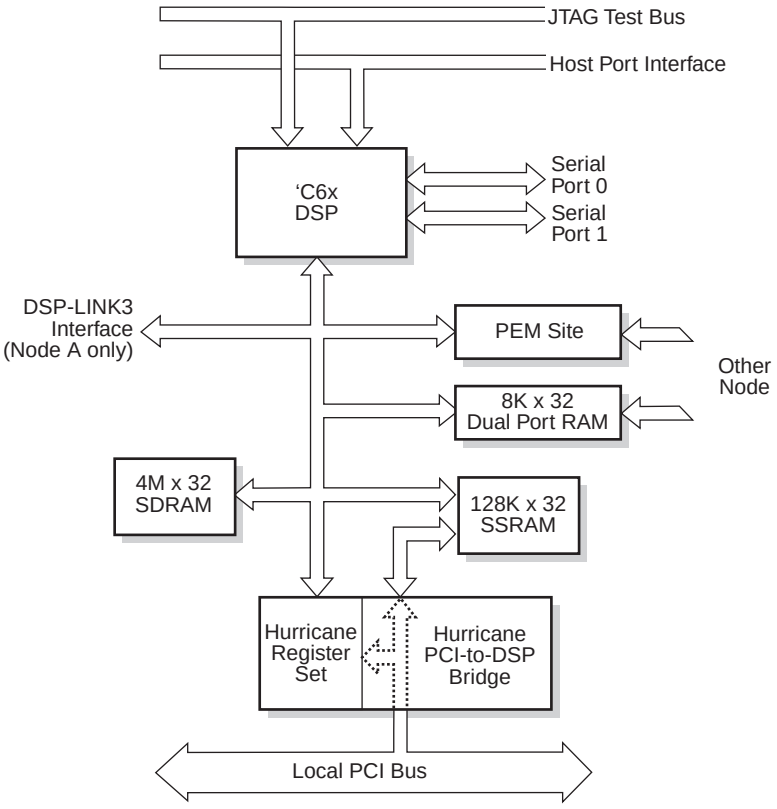


Figure 10 DSP Node Resources

3.1. Processor Memory Map

Each TMS320C6x DSP processor has a 4 Gigabyte address space consisting of both internal ‘C6x memory and external memory space. The memory space is byte-addressed with 32-bit words aligned on addresses having with their two LSBs equal to “00”, such as 0x0170 0000 and 0x0170 0004. Refer to the TMS320C6x documentation for complete information about this address space.

The ‘C6x internal memory consists of program and data RAM, as well as peripheral registers.

The external memory space is used to access the following external memory resources on the ‘C6x local bus:

- PEM site
- SDRAM
- SSRAM
- Dual-port RAM
- Local Hurricane registers (providing access to the local PCI bus)
- DSP~LINK3 interface (node A only)

The external memory space is partitioned into four memory regions controlled by strobe signals CE0, CE1, CE2, and CE3. External memory resources on the ‘C6x local bus are assigned to one of the four strobe lines. The processor’s boot code sets ‘C6x internal peripheral registers to define the exact size and location of the memory regions assigned to the strobes.

The internal peripheral registers for Daytona must be initialized to the values in the following table upon reset for the board to operate.

Table 6 'C6x Internal Peripheral Register Values

Register *Address*	Value
Global Control Register *0x0180 0000*	0x0000 3078
EMIF CE0 Control Register *0x0180 0008*	0xFFFF 3F43
EMIF CE1 Control Register *0x0180 0004*	0x44B4 D823
EMIF CE2 Control Register *0x0180 0010*	0xFFFF 3F33
EMIF CE3 Control Register *0x0180 0014* (Used for PEM)	0x72B7 0A23
EMIF SDRAM Control *0x0180 0018*	0x0544 A000
EMIF SDRAM Timing *0x0180 001C*	0x0000 061A

The ‘C6x offers two memory map modes as described in the ‘C6x documentation: Memory Map 0 and Memory Map 1. Memory Map 1 is always used with Daytona.

The following memory map gives the location and size of the resources within the ‘C6x memory map on Daytona. Strobe line assignment is shown for Memory Map 1.

Address Range		Size	Description
Start	**End**		
0x0000 0000	0x0000 FFFF	64KB	Internal Program RAM
0x0001 0000	0x003F FFFF	4MB-64KB	reserved
0x0040 0000	0x013F FFFF	16MB	**CE0** (SSRAM)
0x0140 0000	0x017F FFFF	4MB	**CE1** (I/O, boot)
0x0180 0000	0x01BF FFFF	4MB	Internal Registers
0x01C0 0000	0x01FF FFFF	4MB	reserved
0x0200 0000	0x02FF FFFF	16MB	**CE2** (SDRAM)
0x0300 0000	0x03FF FFFF	16MB	**CE3** (PEM)
0x0400 0000	0x7FFF FFFF	2GB-64MB	reserved
0x8000 0000	0x8000 FFFF	64KB	Internal Data RAM
0x80001000	0x803F FFFF	4MB-64KB	reserved
0x8040 0000	0xFFFF FFFF	2GB-4MB	reserved

Figure 11 'C6x Memory Map

As can be seen, the SSRAM corresponds to strobe CE0, the SDRAM to CE2, and the PEM site to CE3. The following I/O and boot resources are assigned to CE1:

- Processor node control and status registers
- Processor node Hurricane registers
- Dual-Port RAM
- DSP~LINK3 interfaces (node A only)
- PEM boot ROM (if supplied on an installed PEM module)

The memory maps for the external resources assigned to CE1 are shown in the following memory map. Because only node A supports the DSP~LINK3 interface, CE1 memory maps are given for the processors on nodes A and B. ‘C6x addresses are provided for the Memory Map 1 only.

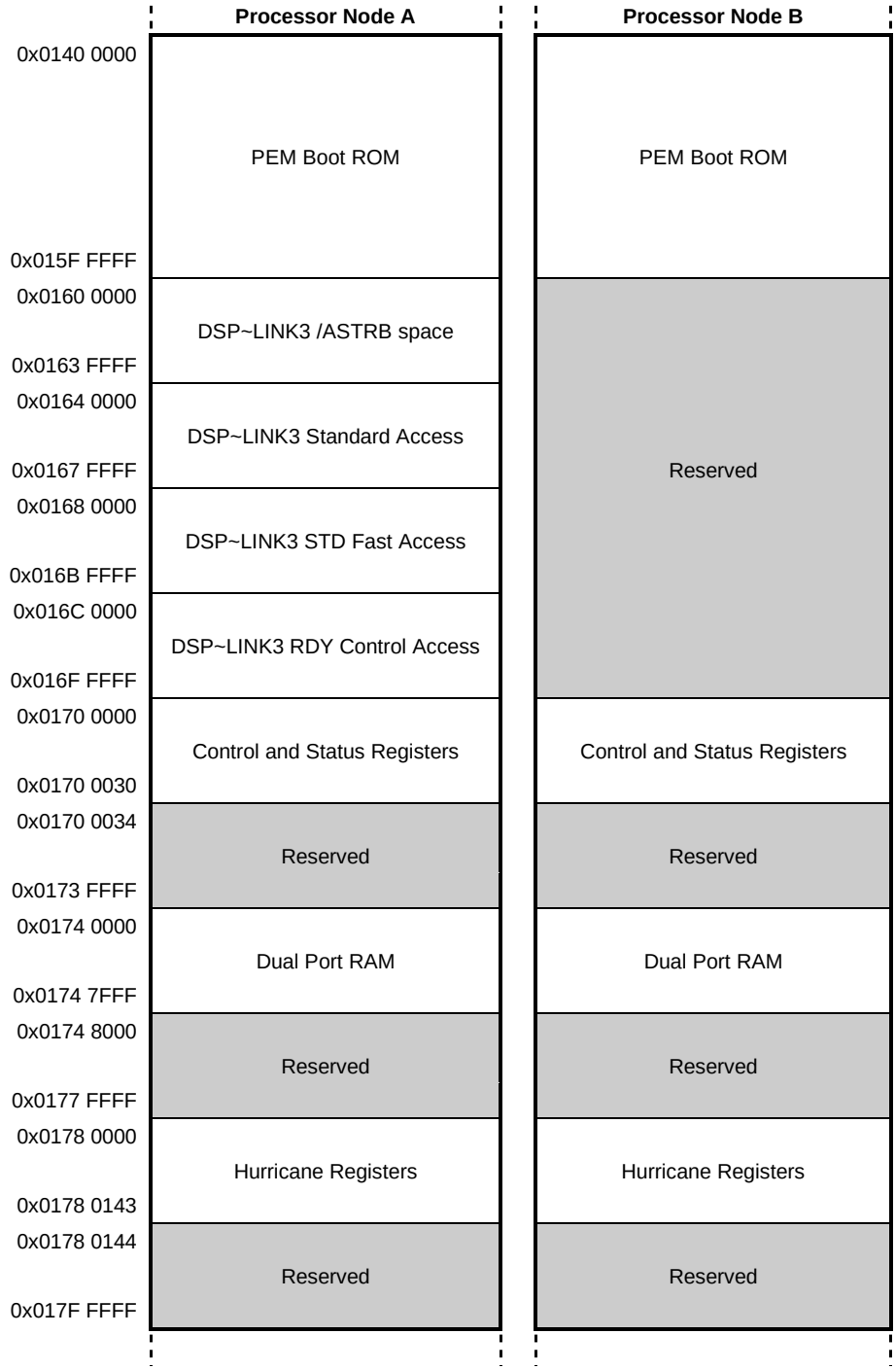


Figure 12 External CE1 Memory Maps

3.2. Processor Booting

The ‘C6x can boot from either the PCI bus (via its Host Port Interface (HPI) port) or from an 8-bit EEPROM on an installed PEM module. The boot source is selected by DIP switch SW3-1. Normally, the processors boot from the HPI port. Setting SW3-1 to the default OFF position selects the HPI as the boot source; setting it to ON selects a ROM boot source.

3.3. Data Transfers From the Processor Node

There are several ways to transfer data from a Daytona processor node. Interrupt signaling can be used to control data transfer for each method. Signal messaging for data transfers can be implemented through interrupts.

- High throughput data transfers from the SSRAM of one processor node to the SSRAM of another are accomplished via Hurricane DMA transfers along the local PCI bus. Data transfer completion can be signaled through the **SSI Interrupt Register** of the destination node.
- Low-latency messaging passing between ‘C6x processors is provided by shared access to the Dual Port RAM. The global interrupts could be configured and used to signal data transfer completion.
- High throughput data transfers from the SSRAM of a processor node to another PCI device (such as the PMC site or PCI host) are accomplished via Hurricane DMA transfers to the PCI device. PCI interrupts can be used to signal data transfer completion to a PCI host. However, the interrupt could arrive before the data transfer is complete because the interrupts do not follow the same path as the data. The system design must take this into account to prevent this from happening.
- Data transfers from the SSRAM of one processor node to anywhere in the ‘C6x address space of another node are accomplished via Hurricane DMA transfers to the HPI port accessed via Hurricane X. When mapped memory pages are used for this, the data transfer completion can be signaled by setting the HINT bit of the destination page’s **HPI Control Register**.

A destination can signal the processor node that is transferring data from its SSRAM by generating an EINT4 interrupt to the source’s ‘C6x. This interrupt is generated through the source processor node’s Hurricane register set. Refer to the *Hurricane Data Sheet* for further information about generating interrupts.

The processor nodes can also transfer data from the ‘C6x serial ports or through PEM modules designed for data transfer. Further information about the Dual Port RAM and Hurricane DMA data transfers can be found in the following sub-sections.

These data transfer modes are shown in the following diagrams.

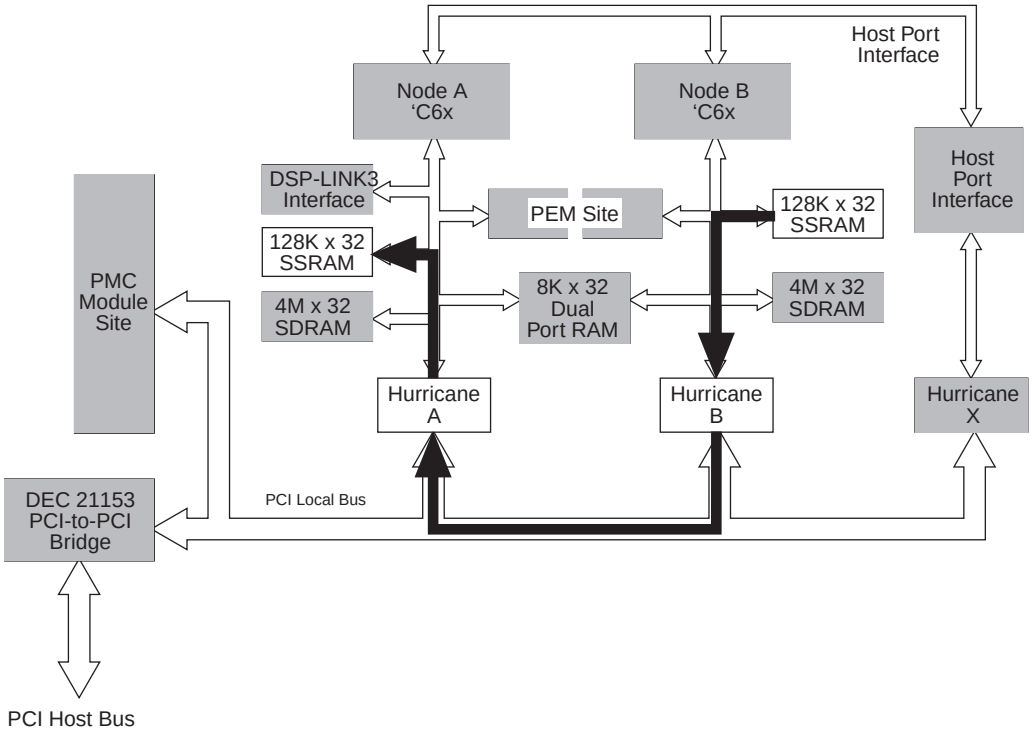


Figure 13 SSRAM to SSRAM Data Transfer Using Hurricane DMA

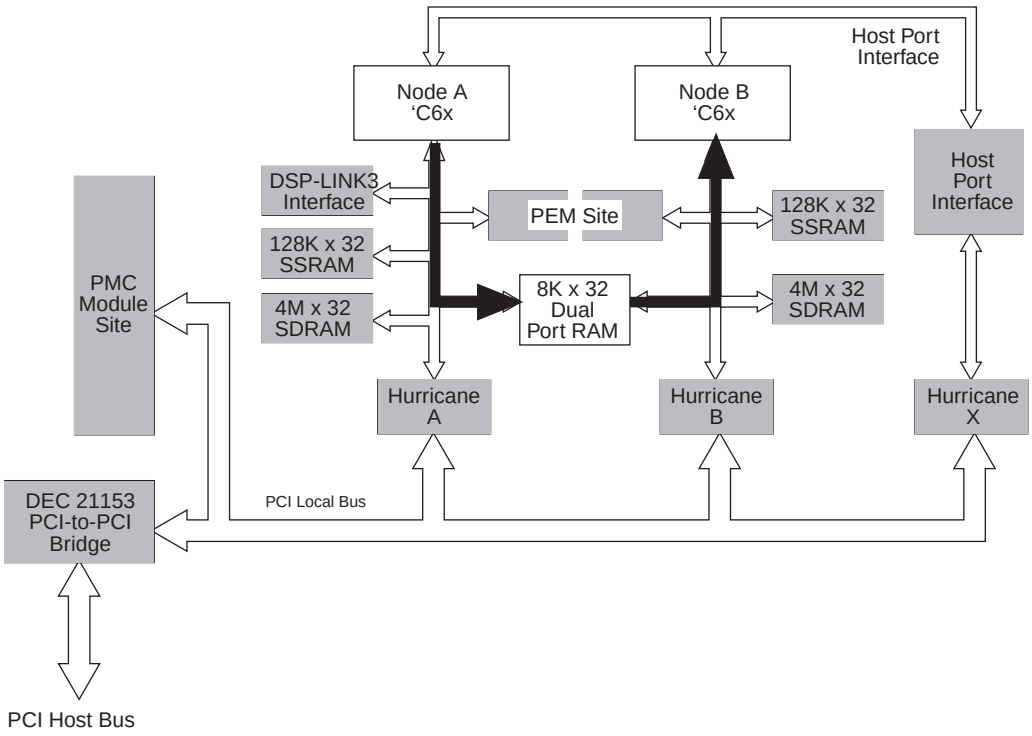


Figure 14 DSP to DSP Data Transfer Using Dual Port RAM

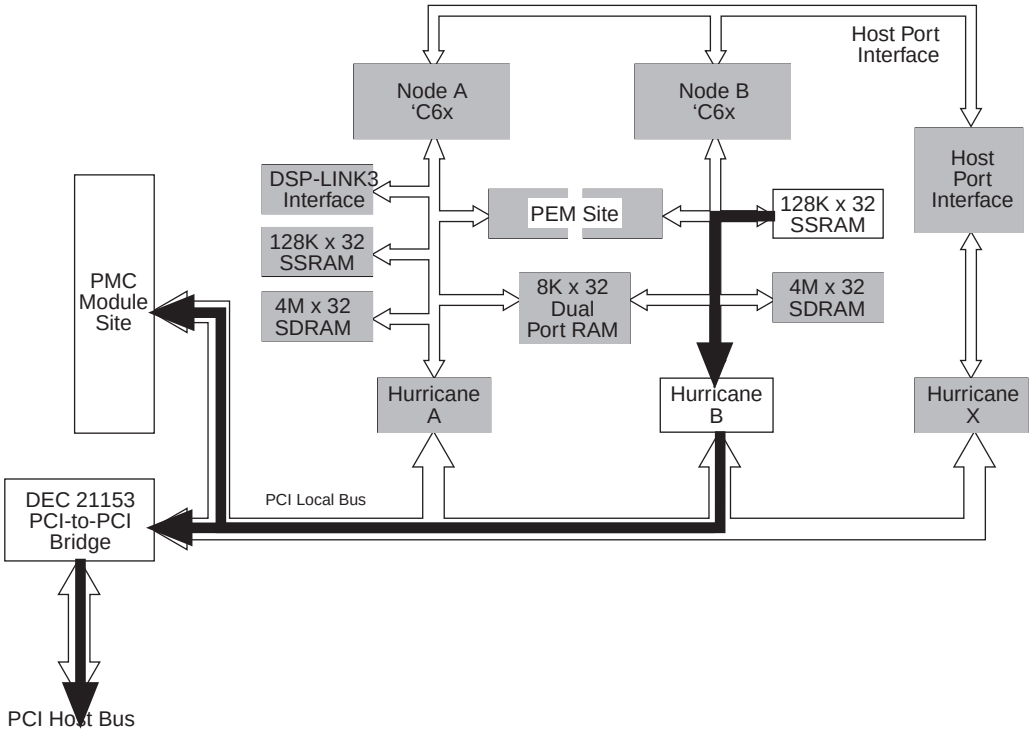


Figure 15 SSRAM to PCI Data Transfer Using Hurricane DMA

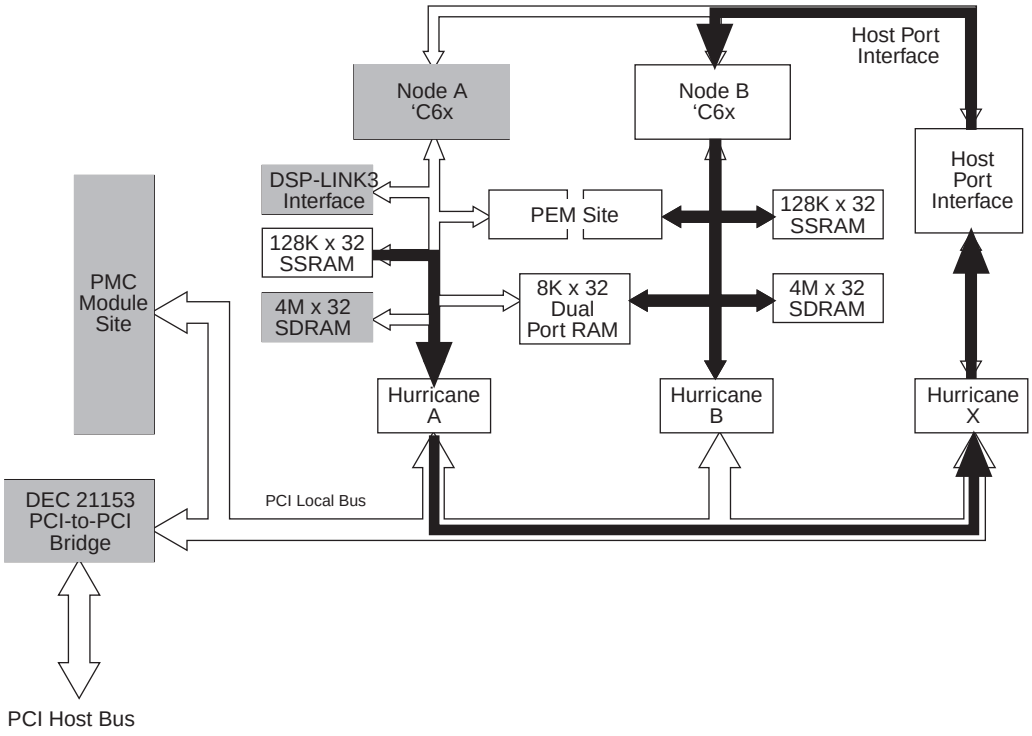


Figure 16 SSRAM to DSP Data Transfer Using Hurricane DMA and HPI

3.4. ‘C6x Serial Ports

Each ‘C6x has two serial ports: serial port 0 and serial port 1. These ports can be routed to the corresponding serial port of the other ‘C6x, the PEM site, and the PMC site. Serial port 0 of each processor can also be routed to an external connector on the Daytona.

The Daytona **Serial Port register** controls how the serial ports are routed. This register is accessible from a PCI host through Hurricane X at PCI offset address 0x0008 0014. Pinouts for the external serial port connectors are provided in section 12.5, *‘C6x Serial Port Connectors*.

3.5. Synchronous SRAM

Each processor node has 512 KB (128K x 32) of Synchronous SRAM. The SSRAM can also be accessed from the local PCI bus through the node’s Hurricane chip. Read and write accesses each require 2 CLKOUT1 cycles within a burst. Each CLKOUT1 cycle is 5 ns at 200 MHz and 4.18 ns at 167 MHz. A PCI host can interrupt the ‘C6x via the **SSI Interrupt register** to signal memory transactions between the PCI bus and the SSRAM. This register is accessible from the PCI bus through the node’s Hurricane chip at PCI address offset 0x0018 0000.

Note: Although, Texas Instruments documentation defines the memory assigned to this address region of the ‘C6x as SBSRAM (Synchronous Burst SRAM), the term SSRAM is used in Daytona documentation.

3.6. Synchronous DRAM

Each processor node has 4M x 32 of synchronous DRAM. Read and write accesses each require 2 CLKOUT1 cycles. Each CLKOUT1 cycle is 5 ns at 200 MHz and 4.18 ns at 167 MHz. An additional 4M x 32 synchronous DRAM per DSP can also be supported on a PEM module.

Note: The synchronous DRAM is *not* shared with the Hurricane PCI interface.

3.7. Processor Expansion Module

The CE3 address space between 0x0300 0000 and 0x03FF FFFF of each ‘C6x is mapped to the PEM (Processor Expansion Module) site. Each PEM site supports two of these 16M ‘C6x processor address spaces; a pair of PEM connectors is dedicated to each ‘C6x. The PEM site provides a simple and flexible interface from the DSP to custom I/O interface hardware. While two DSPs share the same PEM, their buses are kept separate. PEM modules are capable of supporting very fast data transfers.

The PEM is capable of booting the DSPs from local ROM, with a 512K x 8-bit boot space available to each DSP between 0x0140 0000 and 0x015F FFFC of the CE1 address space. It is not within the CE3 space used by the rest of the PEM in the CE3 address space. DIP switch SW3-1 selects the board’s boot mode.

Refer to the *Processor Expansion Module Specification* for mechanical and functional details of the PEM interface.

3.8. Host Port Interface

The Host-Port Interfaces of all DSP processors are connected to a single HPI interface device connected to Hurricane X. This interface is the primary host control interface. This interface can be used for downloading code and as a control path from the host to the DSP.

Through this interface, any master on the local PCI bus can access all the resources seen on the ‘C6x processor bus; the entire ‘C6x memory is accessible. Refer to the PCI Bus Interface chapter for complete information about how ‘C6x address space access is implemented on Daytona.

3.9. Interrupt Lines

There are four external interrupt inputs on the ‘C6x. They are EINT4, EINT5, EINT6, and EINT7. Refer to the *Interrupt Handling* chapter for information about how these interrupts are used on Daytona.

3.10. Dual-Port RAM

An 8K by 32-bit (32 Kbyte) block of dual-port RAM provides low-latency message-passing between the ‘C6x processors on Daytona. Read accesses require 31 CLKOUT1 cycles; write accesses require 25 CLKOUT1 cycles. Each CLKOUT1 cycle is 5 ns at 200 MHz and 4.18 ns at 167 MHz. This memory is simultaneously accessible to each DSP in the ‘C6x address range 0x0174 0000 and 0x0174 7FFC.

The dual-port RAM only supports 32-bit word accesses; byte accesses are not supported.

Concurrent access to the same location within the dual-port RAM by two processors can produced indeterminate results. The following table describes the results of the different concurrent access situations that can occur.

Table 7 Concurrent Dual-Port RAM Accesses

Node A		Node B	
Result	**Operation**	**Operation**	**Result**
OK	Read	Read	OK
Indeterminate	Read	Write	OK
OK	Write	Read	Indeterminate
Indeterminate	Write	Write	Indeterminate

3.11. Local Hurricane Register Interface

The SSRAM of each processor node is connected to the PCI bus of the board through the node's local Hurricane PCI-to-DSP bridge chip. The Hurricane is seen as a PCI device on this PCI bus.

Note: The Hurricane does ***not*** provide any access to the local SDRAM, DSP~LINK3, or to any local DSP resource from the PCI bus, except to the SSRAM.

The DSP node Hurricane uses a serial EEPROM for initialization. The EEPROM defines the basic operation of the Hurricane and should not be modified.

A node's SSRAM can be read and written from the PCI bus through the Hurricane chip. The Hurricane DMA controller can be used to perform DMA transfers between the node's SSRAM and any other destination on the local PCI bus, such as the SSRAM on another node or a destination on the host PCI bus. The local SSRAM starts at the Hurricane's base address for CS0 accesses.

A bus master on the PCI bus can also use the **SSI Interrupt register**, at PCI offset 0x0018 0000 from the Hurricane BAR0 base address, to generate an HPI interrupt on the 'C6x by setting one of 8 bits in this register. In addition to generating the HPI interrupt, a corresponding bit within the node's **HPI Interrupt register** is also set. Software applications can use these registers to implement interrupt-driven messaging when transferring data to and from the node's SSRAM.

Both the 'C6x DSP and the local PCI bus can read and write registers within the Hurricane chip. The Hurricane specific register set controls and monitor Hurricane operations such as SSRAM DMA transfers. The PCI configuration register block of the Hurricane can also be read by the 'C6x.

Note: Do not write to the PCI configuration register block from the 'C6x at any time. Although the Hurricane's PCI configuration register block can be seen by the 'C6x, it must be considered a reserved location in memory. Writing to this space can cause PCI system crashes and other problems.

Addresses and descriptions of the registers are given in the following tables.

Table 8 Processor Node Hurricane Register Access

PCI Offset	'C6x Address	Short Name	Register
0x0010 0000	0x0178 0000	DCSR	DMA Control / Status Register
0x0010 0004	0x0178 0004	IFSC	Interrupt Flag, Set, Clr
0x0010 0008	0x0178 0008	IED	Interrupt Enable to DSP
0x0010 000C	0x0178 000C	IEP	Interrupt Enable to PCI
0x0010 0010	0x0178 0010	IT	Interrupt type
0x0010 0014	0x0178 0014	GCSR	General control and status register
0x0010 0018	0x0178 0018	TTP	Timer trigger point
0x0010 001C	0x0178 001C	TV	Timer value
0x0010 0020 to 0x0010 003C	0x0178 0020 to 0x0178 003C		Reserved registers: Do **not** modify.
0x0010 0040	0x0178 0040	DDA	DSP Address
0x0010 0044	0x0178 0044	DPA	PCI Address
0x0010 0048	0x0178 0048	DLNGTH	Length
0x0010 004C	0x0178 004C	DINTP	Interrupt Point
0x0010 0050	0x0178 0050	DSTRD	DSP Stride
0x0010 0054	0x0178 0054	DPC	Packet Control
0x0010 0058	0x0178 0058	DCAR	DMA Chain Address Register
0x0010 005C	0x0178 005C		Reserved register: Do **not** modify.
0x0010 0060	0x0178 0060	DCDA	Current DSP Address
0x0010 0064	0x0178 0064	DCPA	Current PCI Address
0x0010 0068	0x0178 0068	DCLNTGH	Current Length
0x0010 006C	0x0178 006C	DBC	PCI DMA burst control
0x0010 0070	0x0178 0070	DFC	DMA FIFO Control
0x0010 0074	0x0178 0074	DBE	PCI byte enable and command register
0x0010 0078	0x0178 0078		
0x0010 007C	0x0178 007C		
0x0010 0080 to 0x0010 00F0	0x0178 0080 to 0x0178 00F0		Reserved registers: Do **not** modify.
0x0010 00F4	0x0178 00F4	DBT	DSP bus hold / wait
0x0010 00F8	0x0178 00F8	DBIC	DSP bus interface control
0x0010 00FC	0x0178 00FC		Reserved register: Do **not** modify

Table 9 Processor Node Hurricane PCI Configuration Register Access

'C6x Address	**31** **16**	**15** **0**
0x0178 0100	Device ID = **0xDA62**	vendor ID = **0x12FB**
0x0178 0104	Status	command
0x0178 0108	Class Code	Revision ID
0x0178 010C	not supported / Header Type	Latency Timer / not supported
0x0178 0110	Base Address Register (BAR0)	
0x0178 0114	not supported	
0x0178 0118	not supported	
0x0178 011C	not supported	
0x0178 0120	not supported	
0x0178 0124	not supported	
0x0178 0128	not supported	
0x0178 012C	Subsystem ID	subsystem Vendor ID
0x0178 0130	not supported	
0x0178 0134	reserved	
0x0178 0138	reserved	
0x0178 013C	Max_Lat / Min_Gnt	Interrupt Pin / Interrupt Line
0x0178 0140	BAR0 Shadow Register	

3.12. Hurricane DMA Data Transfers

The 'C6x can initiate PCI bus master transfers using the DMA controller on its local Hurricane. The DMA controller is controlled through the Hurricane's internal registers. Refer to the *Hurricane datasheet* and the *Daytona Programming Guide* for further information on using this feature.

3.13. Hurricane DSP Bus Bandwidth

The amount of time, or bandwidth, that the Hurricane can own the ‘C6x bus can be restricted using the **DSP Bus Hold / Wait register** (DBT) located within each node’s Hurricane chip. The bus bandwidth can therefore be customized for specific Daytona applications. The register can be accessed from the PCI bus at offset 0x0010 00F4 from the Hurricanes BAR0 address, or from the node’s ‘C6x at address 0x0178 00F4.

The **DSP Bus Hold / Wait register** configures the DSP Bus Bandwidth Timer. This timer allows an upper limit on the bandwidth that the Hurricane shares with the ‘C6x. The bandwidth can be set to be unrestricted, or the Hurricane can be given a large portion or small fraction of the bandwidth for the bus it shares with the ‘C6x. In addition to limiting the bandwidth, the frequency that the Hurricane releases the bus to the ‘C6x can be programmed. The Hurricane can be programmed to release the bus frequently, or to keep for extended periods.

Upon reset of the Daytona, the **DSP Bus Hold / Wait register** is set to the default Hurricane value of 0x0000 0000, which gives the Hurricane unrestricted bandwidth to the ‘C6x DSP bus. Refer to the *Hurricane Data Sheet* for further information on this register and how to configure it.

4 PEM Interface

A PEM site is provided supporting a 16M address spaces for each ‘C6x processor. Each processor has a dedicated pair of PEM connectors on the PEM site. The PEM site provides a simple and flexible interface from the DSP to custom I/O interface hardware. While two DSPs share the same PEM, their buses are kept separate. The following figure shows the location of the PEM interface.

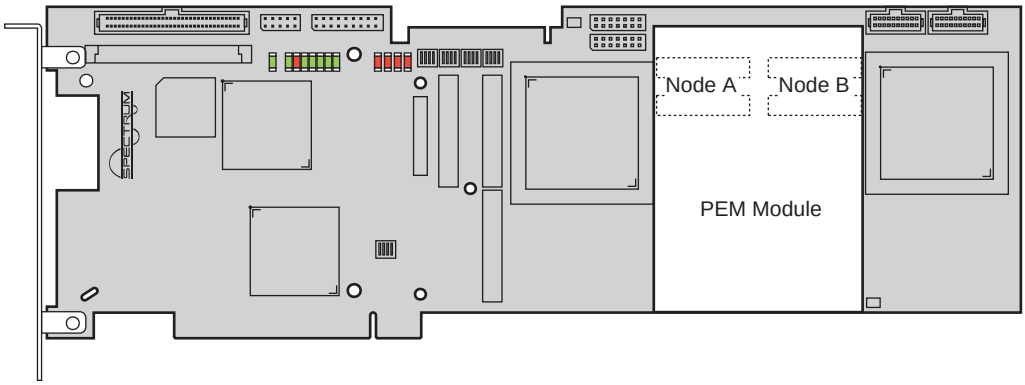


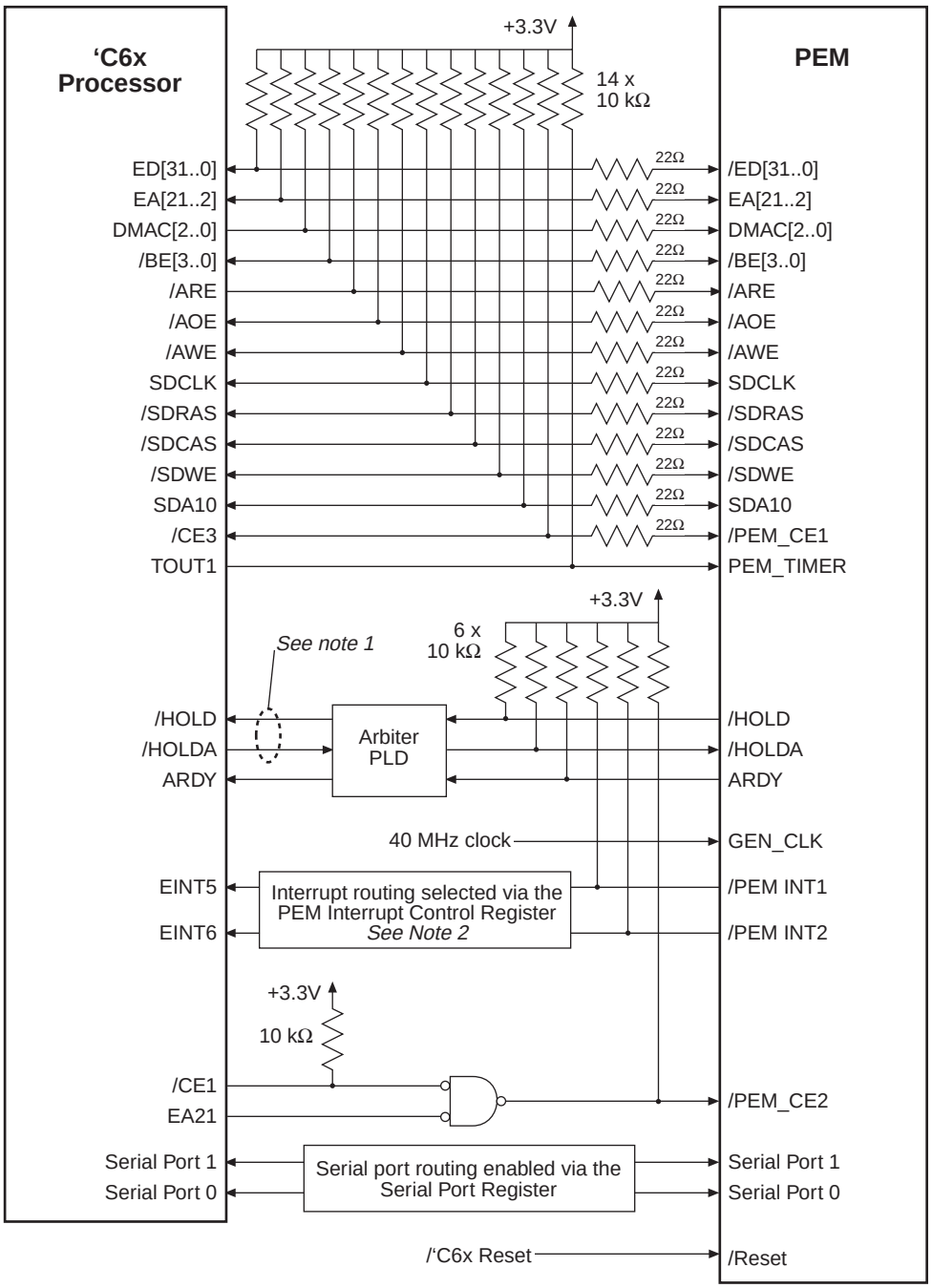
Figure 17 PEM Module Location

Mechanical and functional details of the PEM interface can be found in the *Processor Expansion Module Specification.*

Each of the PEM interrupts (PEM INT1 and PEM INT2) can be routed to either EINT5 or EINT6 of its corresponding ‘C6x under control of the **PEM Interrupt Control Register**. This register is located at address 0x0170 000C of each ‘C6x processor’s address space.

The serial ports of each ‘C6x can be routed to the PEM interface by each DSP through the **Serial Port Register**. This register is accessed from the PCI bus at offset 0x0008 0014 from the BAR0 address of Hurricane X.

The following schematic shows the PEM interface between each Daytona ‘C6x processor and its connectors on the PEM site.



Notes

Note 1: /HOLDA must be released before /HOLD can be asserted, and /HOLDA must be asserted before /HOLD can be released.

Note 2: The PEM interrupts are inverted before being routed to the 'C6x EINT pins.

Figure 18 PEM Interface Schematic

5 PMC Interface

A PMC site is provided supporting PMC Module mechanical and electrical specifications. On the Daytona local PCI bus, the PMC site appears as device 0. Refer to the PMC specification for further information. The following figure shows the location of the PMC interface.

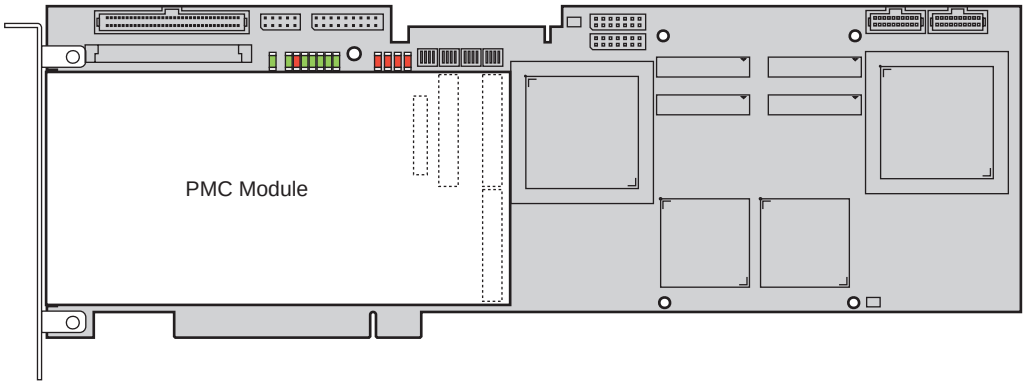


Figure 19 PMC Module Location

The INT# interrupts from the PMC site can be routed to their respective interrupts on the host PCI bus. They can also be routed the EINT6 pin of the ‘C6x processors. Two DIP switches are used to route the four PMC interrupts. SW3-2 routes PMC INTB#, INTC#, and INTD#, and SW3-3 routes PMC INTA#.

A ‘C6x can control and monitor these interrupts through the **PMC Interrupt Status Register** and the **PMC Interrupt Control Register**.

See the following sections for further information on the PMC site:

- section 1.6, *DIP Switch Settings*
- section 2.1, *DEC 21153 Host PCI Interface*
- section 8.7, *PMC Interrupts*

A non-standard PMC connector, JN5, is included on the PMC site. The exact location of this connector is shown in the following diagram. The AMP 5-316466-0 connector that is used on for JN5 does not violate the PMC component area stated in the PMC specifications.

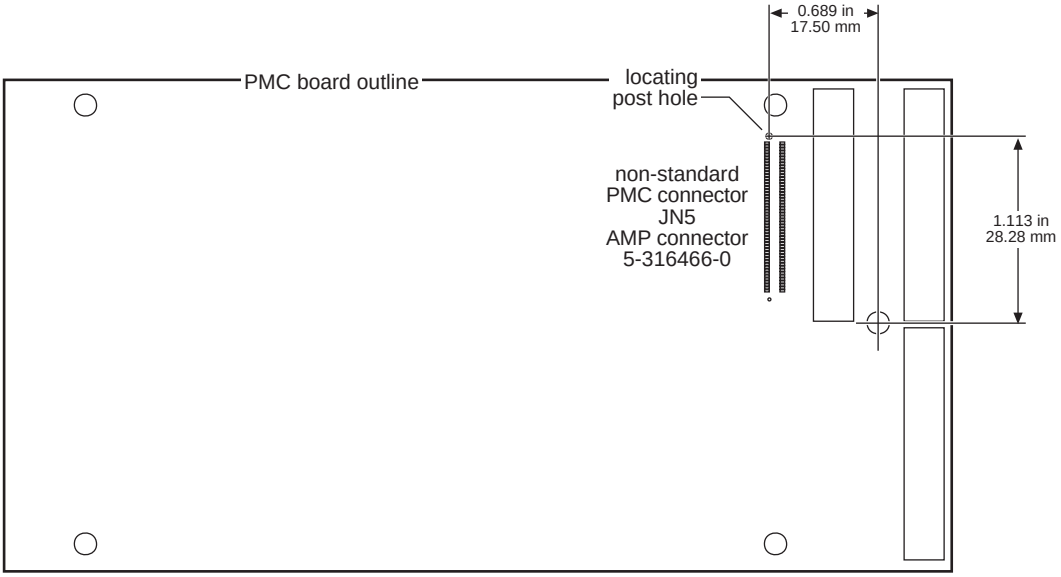


Figure 20 JN5 Connector Location

6 DSP~LINK3 Interface

Up to 4 slave DSP~LINK3 I/O modules can be attached to the Daytona through the ribbon cable connector or by the mezzanine connector. The ribbon cable can be up to 12 inches (30 cm) long. Both connectors can be used at the same time. The following figure shows the location of the DSP~LINK3 interface.

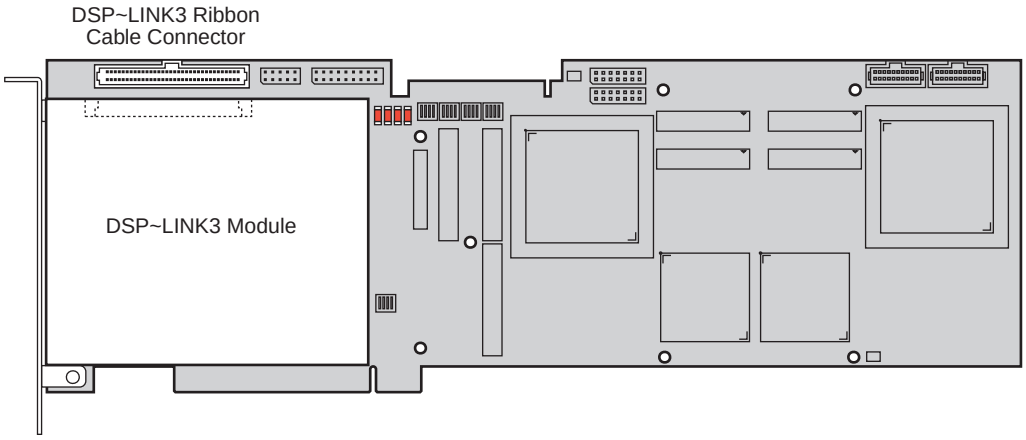


Figure 21 DSP~LINK3 Module and Connector Location

6.1. DSP~LINK3 Operating Modes

The Daytona supports the three data transfer modes and the address page turn (/ASTRB) cycle of the DSP~LINK3 interface in four 64K address spaces accessed from the CE1 memory page of the node A ‘C6x. Each mode is assigned its own 64K memory space.

The following table shows how the DSP~LINK3 operating modes are accessed from the ‘C6x on node A.

Table 10 DSP~LINK3 I/O Map

Start Address	Cycle Type	Description
0x0160 0000	ASTRB	Generates an ASTRB cycle. The address on A17:A2 is written to the ASTRB latch on the DSP~LINK3 device. For slave boards that require more than the 16 KWords of addressing provided by the standard DSP~LINK3 address lines. The bus master uses the /ASTRB cycle to place the page address onto the DSP~LINK3 data lines. It determines which address page is accessed on the slave board. This allows access to up to 2^{14} address pages with each address page having an address depth of 2^{14}. The /ASTRB Cycle has the same timing as the Standard Fast transfer cycle.
0x0164 0000	Standard	Generates a DSP~LINK3 I/O read/write cycle with STANDARD timing. For slave boards that are similar to DSP~LINK1 slave boards and operate with a fixed, minimum 260 ns access time.
0x0168 0000	Fast	Generates a DSP~LINK3 I/O read/write cycle with FAST timing. For DSP~LINK3 slave boards that have fast, fixed 140 ns access time. This memory space is shared with the Address Strobe Control operating mode.
0x016C 0000	RDY	Generates a DSP~LINK3 I/O read/write cycle with /RDY timing. For DSP~LINK3 slave boards that require variable length access times. /DSTRB is active until the slave asserts the DSP~LINK3 ready signal (/RDY) to end the cycle.

The ‘C6x physical address bits A17..A2 are mapped to the DSP~LINK3 address bits A15..A0, so address 0x0164 0000 corresponds to DSP~LINK3 address 0x0000, 0x00164 0004 will correspond to 0x0001, and so on.

Refer to the *DSP~LINK3 interface specification* for complete timing information for the four address pages.

6.2. Interface Signals

The DSP~LINK3 interface consists of the following interface signals:

- 32 data I/O lines: D[31..0]
- 16 address outputs: A[15..0] A15 and A14 are used for slave device (board) selection.
- /DSTRB, /ASTRB, R/W and /RST outputs
- Tri-state ready (/RDY) input
- 4 interrupt inputs (INT0 to INT3). These interrupts are routed to the EINT5 line of node A’s ‘C6x. They can be individually enabled through the **DSP~LINK3 Control register** accessible to the node A ‘C6x at address 0x170 0018.

The control signals are terminated via a SCSI terminator. Refer to *DSP~LINK3 Specification* for details (available from Spectrum’s internet web site at http://www.spectrumsignal.com)

6.3. Resetting the DSP~LINK3 Interface

The DSP~LINK3 interface can be reset by writing a ‘1’ to the DL3_RST bit (bit D4) of the **DSP~LINK3 Control Register**. This register is accessible in the address space of the ‘C6x on node A at address 0x0170 001C. Upon board reset, this bit is automatically set to ‘1’; resetting the DSP~LINK3 interface.

7 JTAG Debugging

The Daytona supports JTAG debugging externally through an XDS510 or equivalent debugger connected to its JTAG connectors, and on-board from its built-in 74ACT8990 Test Bus Controller (TBC)

When an external XDS is connected to the JTAG IN connector (J14), the Daytona detects the presence of the TCK line and disconnects the on-board TBC from the JTAG chain. External JTAG remains selected until power on reset.

For on-board JTAG debugging, a PCI bus master accesses the TBC through Hurricane X. The TBC is located between address 0x0000 0000 and 0x0000 FFFC of Hurricane X's PCI memory space.

The 'C6x must be out of its reset state before JTAG debugging is started. The **`sysload.exe`** example program supplied with the Daytona Software Development Kit (SDK) can be used to reset the 'C6x. Upon completion, the program leaves the 'C6x out of its reset state.

The JTAG connectors supports both 5 Volt and 3.3 Volt JTAG connections.

> **Note:** The DSPINT bit of the processor's HPIC register must be set to "1" before code is downloaded to the DSP. If not, the processor will not boot properly and the debugger won't run properly in HPI boot mode.

The JTAG chain is shown in the following diagram.

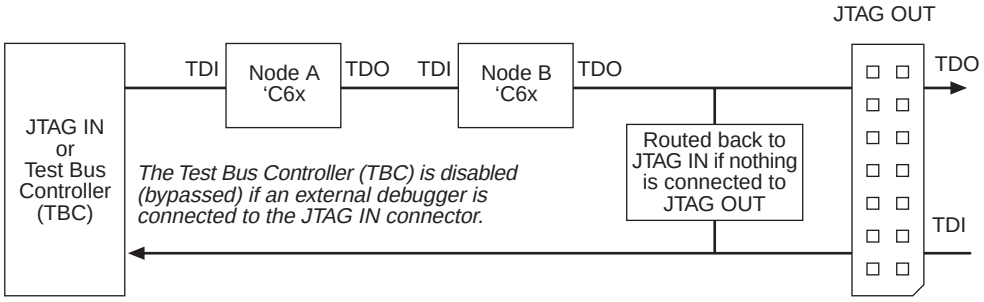


Figure 22 JTAG Chain

The JTAG IN input is buffered to reduce the load on an external JTAG device. The JTAG OUT output is buffered to guarantee enough drive to external JTAG loads.

Several Daytonas can be daisy-chained together through their JTAG connectors for multi-board debugging. The JTAG cable of the external debugger should only be connected to the JTAG IN of the first board. The JTAG OUT of the first board should be

connected to the JTAG IN of second board. The JTAG OUT of the second board should be connected to the JTAG IN of third board and so on. See the following figure.

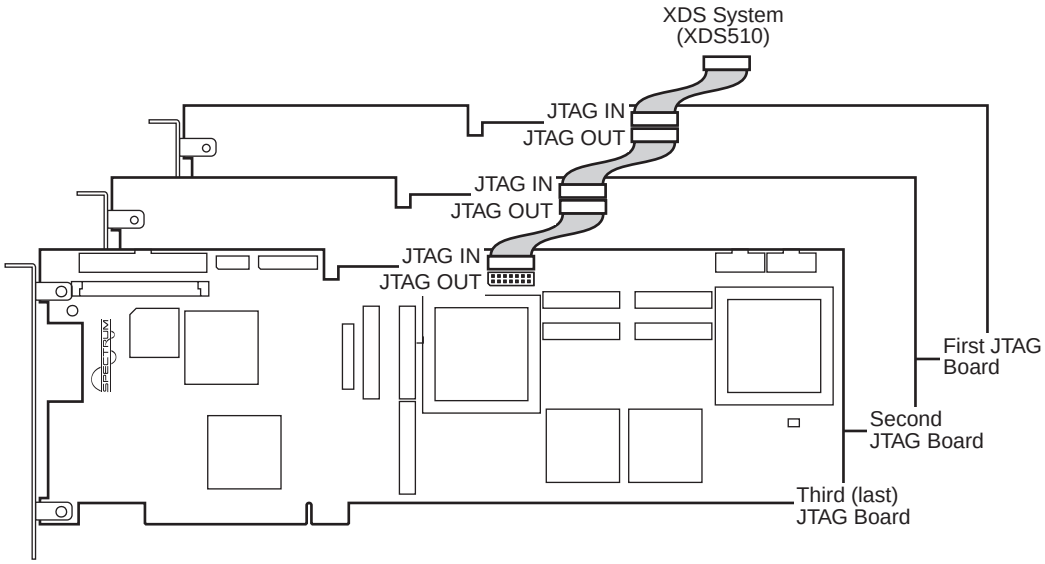


Figure 23 Multi-board JTAG Connections

Note: All hardware should be powered off before the JTAG cables are connected and the JTAG chain is set up.

8 Interrupt Handling

8.1. Overview

The ‘C6x has four interrupt pins which are configurable as either leading or falling edge-triggered interrupts. For the Daytona these interrupts are configured as falling edge-triggered interrupts. The /NMI interrupt is not used and is tied high.

The following table shows how interrupts are routed to these pins on the Daytona.

Table 11 Interrupts to the 'C6x DSPs

Interrupt	Source	Description
HINT*	HPI Interrupts	Generated by a PCI host through Hurricane X for mapped HPI memory page operation
	SSI Interrupts	Generated by a PCI host through the DSP’s local Hurricane for SSRAM access
EINT4	Local Hurricane chip	Generated by registers within the Hurricane local to the DSP
EINT5	PEM Interrupts	INT1 and INT2 interrupt lines from the PEM site
	DSP~LINK3 Interrupts (Node A only)	INT0, INT1, INT2, and INT3 from the DSP~LINK3 connector
EINT6	PMC Interrupts	INTA#, INTB#, INTC#, and INTD# interrupts from the PMC site
	PEM Interrupts	INT1 and INT2 interrupt lines from the PEM site
EINT7	Global Interrupts	General purpose interrupt lines routed from an external connector or between the DSPs

*HINT, in this context, is the Host port host to DSP Interrupt.

Interrupts can also be generated to the host PCI bus from the Hurricane chips on the Daytona. Each Hurricanes has its PCI_INT line routed to the following interrupts on the host PCI bus.

Hurricane	Host PCI Interrupt
Hurricane X (System)	INTC#
Hurricane A	INTD#
Hurricane B	INTA#

Refer to the *Hurricane Datasheet* for further information on the Hurricane interrupts.

8.2. HPI Interrupts to the ‘C6x

HPI interrupts can be generated by any PCI bus master through the Hurricane X. These interrupts are intended for mapped HPI memory page operation. The interrupt is generated by writing a ‘1’ to one of the **DSPINT** bit of the memory page’s **HPI Control Register**. This causes an HINT interrupt to the ‘C6x and sets the appropriate bit in the processor node’s **HPI Interrupt** register. Table 13 Mapped HPI Page Register , in section 2.5, provides the addresses of the **HPI Control Registers.** See section 2.5, *“Mapped HPI Pages”*, for complete information on mapped HPI pages.

To clear HPI interrupts generated from the PCI bus through the **HPI Control register**, the ‘C6x must first clear this interrupt internally by writing a ‘1’ to the DSPINT bit of its internal **HPI Control register** (HPIC). This register is located within the processor at internal ‘C6x address 0x0188 0000. The ‘C6x can then access its **HPI Interrupt register** (at 0x0170 0000 in the ‘C6x address space) to identify and clear the HPI interrupt.

8.3. SSI Interrupts to the ‘C6x

SSI interrupts can be generated by any PCI bus master through the DSP’s local Hurricane. These interrupts are intended for **SS**RAM (**I**nterrupt) access operations. A PCI device can generate this interrupt by writing a ‘1’ to one of the 8 SSI bits of the **SSI Interrupt register**. This register is located at offset 0x0018 0000 from the processor node’s Hurricane BAR0 address. This causes an HINT interrupt to the ‘C6x and sets the appropriate bit in the processor node’s **HPI Interrupt register**.

To clear HPI interrupts generated through the **SSI interrupt register**, the ‘C6x must first internally clear this interrupt by writing a ‘1’ to the DSPINT bit of its internal **HPI Control register** (HPIC). This register is located within the processor at internal ‘C6x address 0x0188 0000. The ‘C6x can then access its **HPI Interrupt register** (at 0x0170 0000 in the ‘C6x address space) to identify and clear the SSI interrupt.

This interrupt can be used by software applications for interrupt-driven messaging involving data transfers to the node’s SSRAM.

8.4. Local Hurricane Interrupts to the ‘C6x

The DSP_INT line of each processor node Hurricane is connected to the EINT4 pin of its ‘C6x DSP. Interrupts are generated by registers within the Hurricane local to the DSP. This interrupt is intended for supporting DMA transfers using the node’s Hurricane chip. Refer to the Hurricane datasheet for further information on the Hurricane interrupts.

8.5. PEM Interrupts to the ‘C6x

Each PEM site is shared by two processor nodes, and each node has its own set of PEM interrupts: PEM INT1 and PEM INT2. Each DSP routes and enables these interrupts from the PEM site via the **PEM Interrupt Control Register** (DSP address 0x0170 000C).

This register allows each DSP to route and enable either of the PEM interrupts to its EINT5 or EINT6 interrupt.

The PME interrupt lines are active-low open collector outputs. They are inverted to generated rising edge triggered interrupts at the ‘C6x. The interrupts are not latched and the status of the PEM interrupts cannot be directly detected. Interrupt status should be provided by the PEM module.

Note: If the PEM interrupts are used, they should not be shared on the selected ‘C6x interrupt pin with any other interrupt.

8.6. DSP~LINK3 Interrupts to the Node A ‘C6x

The DSP~LINK3 interrupts are routed to EINT5 of the node A processor. The **DSP~LINK3 Control Register** (node A DSP address 0x0170 001C) enables the four DSP~LINK3 interrupts: INT0, INT1, INT2, and INT3. Each interrupt corresponds to a bit in this register which, when set to ‘1’, enables that interrupt to generate a low-to-high transition on the ‘C6x interrupt pin EINT5.

Writing ‘0’ to the appropriate bit disables DSP~LINK3 interrupts from EINT5 for the corresponding DSP~LINK3 interrupt. These bits can also be read to determine how the interrupt mask is set. All bits are set to ‘0’ upon reset, disabling all DSP~LINK3 interrupts from reaching EINT5.

To determine which of the four DSP~LINK3 interrupts generated the interrupt on its EINT5 pin, the node A DSP reads the **DSP~LINK3 Interrupt Status Register** (node A DSP address 0x0170 0018). Each of the four DSP~LINK3 interrupts (INT0, INT1, INT2, and INT3) has a corresponding bit in the register. A ’1’ in the bit indicates that the corresponding DSP~LINK3 interrupt has been latched.

The node A DSP also uses the **DSP~LINK3 Interrupt Status Register** to clear the DSP~LINK3 interrupt by writing a ‘1’ to the bits indicating interrupts.

Although DSP~LINK3 interrupts are defined as level-sensitive interrupts, ‘C6x interrupts are edge sensitive. When a high-to-low transition occurs on an enabled DSP~LINK3 interrupt line, a low-to-high transition occurs on ‘C6x EINT5 pin and the interrupt event is latched.

Only interrupts that are specified in the write cycle are cleared when writing to the **DSP~LINK3 Interrupt Status** register. If any interrupt latch remains active, another pulse is generated on EINT5.

8.7. PMC Interrupts

The INTA#, INTB#, INTC#, and INTD# PCI interrupts of the PMC site can be routed to the EINT6 pin of the Daytona's 'C6x processors and to the host PCI bus. Registers for each 'C6x allow the interrupts to be selectively enabled, identified and cleared by each processor. The following two DIP switches on the Daytona route the interrupts to their corresponding interrupts on the host PCI bus.

DIP Switch	PMC to Host PCI Interrupt
SW3-3	INTA#
SW3-2	INTB#, INTC#, INTD#

Caution: Because the DIP switches and registers allow the PMC interrupts to be simultaneously routed to both the host PCI bus and to the 'C6x processors, a conflict may result if both the PCI host and the 'C6x attempt to handle the interrupt. To prevent possible conflict, PMC interrupts that have been routed to the host PCI bus can be disabled from going to the 'C6x processors through the **PMC Interrupt Control register** of each processor, and also disabled from going to the PCI host via the DIP switches.

The four PMC interrupts (INTA#, INTB#, INTC#, and INTD#) are selectively routed to the EINT6 pin of each processor by the processor's **PMC Interrupt Control** register. Each of the four interrupts corresponds to one of four enable bits in this register. Writing a '1' to a bit enables low-to-high transitions to be generated on pin EINT6 for the corresponding PMC interrupt.

Upon receiving an interrupt on its EINT6 pin, a 'C6x processor can determine which PMC interrupt, if any, generated the interrupt by reading its **PMC Interrupt Status** register. Each of the four interrupts corresponds to one of four enable bits in this register. The PMC interrupt causing the EINT6 interrupt will have a '1' in its bit position.

If a PMC interrupt caused the processor's EINT6 interrupt, the processor can clear the interrupt by writing a '1' to the corresponding PMC interrupt bit in the **PMC Interrupt Status** register.

8.8. Interrupts to the Host PCI Bus

Interrupts to the host PCI bus can be generated by the DSPs and by the Hurricane chips. These interrupt sources are mapped to the following PCI interrupt lines.

Interrupt Source	PCI Interrupt Line
DSP A, DSP B, and Hurricane X	INTC#
Hurricane A	INTD#
Hurricane B	INTA#

INTC# interrupts from DSP A, DSP B, and Hurricane X to the PCI host are enabled through the **Interrupt Control Register** at PCI offset 0x0008 000C from the Hurricane X base address 0 (BAR0). Each interrupt source has a corresponding bit in this register. Setting the bit to '1' enables the corresponding source to generate interrupts to the host PCI bus.

When the corresponding PCI interrupts are enabled, a DSP generates an INTC# interrupt to the host by setting the HINT bit (bit D2) of its node's **HPI Control Register** (at DSP address 0x0188 0000) to '1'. Interrupts are generated from the Hurricane chips through the Hurricane register sets. Refer to the *Hurricane Data Sheet* for more information.

The PCI host can determine whether an INTC# interrupt was generated by DSP A, DSP B, or Hurricane X by reading the **Interrupt Status Register** at offset 0x0008 0008 from the PCI base address 0 (BAR0) of Hurricane X.

To clear INTC# interrupts generated by a DSP, the host writes a '1' to the HINT bit of any of the node's **HPI Control Registers**. Hurricane generated interrupts are cleared through the Hurricane registers sets. Refer to the *Hurricane Data Sheet* for more information.

Note: The HPIC register can be accessed from the 'C6x and a PCI host via the HPI. It is organized as a 32-bit register whose high halfword and low halfword contents are the same. When writing to it from the host, both halfwords must be identical.

8.9. Global Interrupts

The Daytona has four global interrupts that provide flexible interrupt capability from

- DSP to DSP
- External device to DSP
- DSP to external devices

These four interrupts are presented as open-collector outputs on connector J10 on the Daytona. A ‘C6x can trigger any of the four interrupt lines using the **Global Interrupt Register** (at DSP address 0x0170 0024). Each interrupt has a corresponding bit in this register. When the interrupts bit is set to ‘1’, an interrupt is generated.

Routing and control of these interrupts is controlled from each processor via registers. A ‘C6x can route and enable one of the four interrupt lines to its EINT7 pin through the **Global Interrupt Select** register (at DSP address 0x0170 0020). This allows an external device, or another ‘C6x, to interrupt the ‘C6x.

By generating an interrupt on a pin that has been routed to the EINT7 pin of another ‘C6x on the board, a ‘C6x can effectively interrupt another ‘C6x. These external interrupt lines can also be used as general-purpose digital I/O pins.

The Global Interrupt lines are 5V TTL compatible lines driven by pseudo-open-collector buffers, and pulled high to 5V with a 10 kΩ resistor.

- Absolute voltages are -0.5 V_{min} and 5.5 V_{max}
- Output low voltage (maximum) is 0.4 Volts
- Input low voltage should be less than 1.0 Volts

9 PCI Addressable Registers

The registers described in this section are accessed by any device on the PCI bus. The registers are summarized in the following table. Addresses for these registers are given as byte offsets from the BAR0 base address of their respective PCI device. (Most registers are accessed from the Hurricane X PCI device.)

Table 12 PCI Addressable Register Summary

Register	PCI Device	Offset	Description
Reset Register	Hurricane X	0x0008 0000	Resets JTAG or the Daytona board
Configuration Register		0x0008 0004	Daytona configuration control and status
Interrupt Status Register		0x0008 0008	PCI interrupt source status
Interrupt Control Register		0x0008 000C	Enables PCI interrupts
Board ID Register		0x0008 0010	Board ID as set by SW2 DIP switch
Serial Port Register		0x0008 0014	Routes the ‘C6x serial ports
HPI Control Register		*0x00C*x* 0000	Host port status and control
HPI Address Register		*0x00C*x* 0004	HPI mapped memory page base address
HPI Mode Register		*0x00C*x* 0010	Reserved
HPI Interrupt Status Register		*0x00C*x* 0014	Status of the HPI interrupt for the page
SSI Interrupt Register (Node A)	Hurricane A	0x0018 0000	Generates an HPI interrupt on the Node A ‘C6x
SSI Interrupt Register (Node B)	Hurricane B	0x0018 0000	Generates an HPI interrupt on the Node B ‘C6x

*Each Mapped HPI Page has one of these registers

The following table provides a complete list of address offsets (from the BAR0 base address of Hurricane X) for each of the four Mapped HPI Page Registers.

Table 13 Mapped HPI Page Register Addresses

Node	Page	HPI Control	HPI Address	HPI Mode	HPI Interrupt Status
Node A	Page 0	0x00C0 0000	0x00C0 0004	0x00C0 0010	0x00C0 0014
	Page 1	0x00C1 0000	0x00C1 0004	0x00C1 0010	0x00C1 0014
	Page 2	0x00C2 0000	0x00C2 0004	0x00C2 0010	0x00C2 0014
	Page 3	0x00C3 0000	0x00C3 0004	0x00C3 0010	0x00C3 0014
	Page 4	0x00C4 0000	0x00C4 0004	0x00C4 0010	0x00C4 0014
	Page 5	0x00C5 0000	0x00C5 0004	0x00C5 0010	0x00C5 0014
	Page 6	0x00C6 0000	0x00C6 0004	0x00C6 0010	0x00C6 0014
	Page 7	0x00C7 0000	0x00C7 0004	0x00C7 0010	0x00C7 0014
Node B	Page 0	0x00C8 0000	0x00C8 0004	0x00C8 0010	0x00C8 0014
	Page 1	0x00C9 0000	0x00C9 0004	0x00C9 0010	0x00C9 0014
	Page 2	0x00CA 0000	0x00CA 0004	0x00CA 0010	0x00CA 0014
	Page 3	0x00CB 0000	0x00CB 0004	0x00CB 0010	0x00CB 0014
	Page 4	0x00CC 0000	0x00CC 0004	0x00CC 0010	0x00CC 0014
	Page 5	0x00CD 0000	0x00CD 0004	0x00CD 0010	0x00CD 0014
	Page 6	0x00CE 0000	0x00CE 0004	0x00CE 0010	0x00CE 0014
	Page 7	0x00CF 0000	0x00CF 0004	0x00CF 0010	0x00CF 0014

Reset Register

Hurricane X BAR0 address + 0x0008 0000

D31..							.. D16
Reserved							
D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	Time-out
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	JTRST	0	Reset

Resets JTAG or the Daytona board.

Reset Resets the HPI interface; all ‘C6x processors; and all control logic circuits, except for the Test Bus Controller. (Read/Write)

- To reset these devices, set this bit to ‘1’
- To release the board from reset, set this bit to ‘0’

Upon power up and a PCI system reset, this bit is set to ‘1’ and the board is held in reset. It remains set to ‘1’ until host software sets it to ‘0’.

JTRST Asserts the JTAG reset TRST signal. (Read/Write)

- To assert the JTAG reset signal, set this bit to ‘1’
- To release the JTAG reset signal from reset, set this bit to ‘0’

Upon power up and a PCI system reset, this bit is set to ‘0’.

Time-out Indicates and clears HPI Time-out condition. All host port accesses are inhibited until this bit is cleared. This bit is ‘0’ upon reset. (Read/Write)

- When set to ‘1’, an HPI time-out has occurred.
- To clear the condition, set this bit to ‘1’

Configuration Register

Hurricane X BAR0 address + 0x0008 0004

D31..							.. D16
Reserved							
D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	ROM	XDS	PMC_PD
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	MAPON

Status and control of Daytona board configuration.

MAPON Enables HPI address translation to provide paged memory access to the ‘C6x processors from the PCI bus. (Read/Write)

- To enable HPI address translation, set this bit to ‘1’. This provides paged memory access to the ‘C6x processors through multiple HPI pages.
- To disable HPI address translation, set this bit to ‘0’. This provides basic HPI access to the ‘C6x processors through a single HPI port.

Upon reset, this bit is set to ‘0’.

PMC_PD Indicates the presence of a PMC module from the Presence Detect line of the PMC interface. (Read only)

- ‘1’ indicates that a PMC module is present.
- ‘0’ indicates that a PMC module is *not* present.

XDS Indicates whether an external debugger is used by detecting the presence of a clock on the JTAG IN TCK line. (Read only)

- ‘1’ indicates that an external debugger is being used.
- ‘0’ indicates that an external debugger is not present.

ROM Indicates whether the ‘C6x will boot from ROM. Determined by the state of the SW3-1 DIP switch. (Read only)

- ‘1’ indicates that the ‘C6x will boot from an 8-bit ROM on a PEM module.
- ‘0’ indicates that the ‘C6x will boot from its HPI port.

Interrupt Status Register

Hurricane X BAR0 address + 0x0008 0008

D31..							.. D16
Reserved							
D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	HINTB	HINTA
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	PCI_X

Indicates the status of the PCI interrupt sources. Represents the logic level of the device's interrupt signal.

- '1' indicates that the interrupt is active.
- '0' indicates that the interrupt is inactive.

PCI_X Hurricane X PCI interrupt

HINTA DSP node A HPI interrupt

HINTB DSP node B HPI interrupt

Interrupt Control Register

Hurricane X BAR0 address + 0x0008 000C

D31..							.. D16
Reserved							
D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	HINTB	HINTA
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	PCI_X

Allows PCI interrupt sources to generate interrupts.

- To allow a PCI interrupt source to generate interrupts, set its corresponding bit to ‘1’.
- To inhibit a PCI interrupt source from generating interrupts, set its corresponding bit to ‘0’.

PCI_X Hurricane X PCI interrupt (This interrupt must also be enabled within the Hurricane X chip register set.)

HINTA DSP node A HPI interrupt

HINTB DSP node B HPI interrupt

Board ID Register

Hurricane X BAR0 address + 0x0008 0010

D31..							.. D16
Reserved							
D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0
D7	D6	D5..					..D0
0	0	Board ID					

Identifies the board according to the Board ID set by DIP switch SW2.

Board ID Bits D[3..0] indicate the Board ID as set by DIP switch SW2. The bits correspond to the following switch positions. Setting a switch to OFF sets its bit to ‘1’.

SW2-1	D3
SW2-2	D2
SW2-3	D1
SW2-4	D0

In systems with multiple Daytona boards, the **Board ID register** allows the PCI host to identify a specific Daytona within the PCI bus. The first four bits of this value (D[3..0]) are set by DIP switch SW2. The upper two bits (D[5..4]) are always ‘0’ for Daytona boards.

Serial Port Register

Hurricane X BAR0 address + 0x0008 0014

D31..							.. D16
Reserved							
D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
SBB1	SBB0	SBA1	SBA0	SAB1	SAB0	SAA1	SAA0

Routes the serial ports from the ‘C6x processors.

SAA[1:0] Routes serial port 0 from DSP A

SAA1	SAA0	Route
0	0	DSP B serial port 0
0	1	PEM Module
1	0	PMC Module
1	1	Serial port connector J15

SAB[1:0] Routes serial port 1 from DSP A

SAB1	SAB0	Route
0	0	DSP B serial port 1
0	1	PEM Module
1	0	PMC Module
1	1	No Connection

SBA[1:0] Routes serial port 0 from DSP B

SBA1	SBA0	Route
0	0	DSP A serial port 0
0	1	PEM Module
1	0	PMC Module
1	1	Serial port connector J16

SBB[1:0] Routes serial port 1 from DSP B

SBB1	SBB0	Route
0	0	DSP A serial port 1
0	1	PEM Module
1	0	PMC Module
1	1	No Connection

HPI Control Register

Address offsets from the PCI base address 0 (BAR0) of Hurricane X for the memory pages on each node								
Node	**Page 0**	**Page 1**	**Page 2**	**Page 3**	**Page 4**	**Page 5**	**Page 6**	**Page 7**
A	0x00C0 0000	0x00C1 0000	0x00C2 0000	0x00C3 0000	0x00C4 0000	0x00C5 0000	0x00C6 0000	0x00C7 0000
B	0x00C8 0000	0x00C9 0000	0x00CA 0000	0x00CB 0000	0x00CC 0000	0x00CD 0000	0x00CE 0000	0x00CF 0000

D31	D30	D29	D28	D27	D26	D25	D24
Reserved – Set to ‘0’s							
D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	FETCH	HRDY	HINT	DSPINT	HWOB
D15	D14	D13	D12	D11	D10	D9	D8
Reserved – Set to ‘0’s							
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	FETCH	HRDY	HINT	DSPINT	HWOB

Provides general status and control of the mapped HPI memory page. Corresponds to the HPIC register of the ‘C6x HPI.

Important! Bits D[31..16] of the HPIC register *must* be programmed with the same values programmed into bits D[15..0], and the HWOB bit must *always* be set to ‘1’ whenever writing to the HPIC register. For example, to set the HWOB bit, write 0x00010001 to this register. Refer to the *TMS320C6201/ C6701 Peripherals Reference Guide* for complete information about the HPI Control Register (HPIC).

HWOB Halfword ordering bit. This bit is shared between the memory pages of the Daytona ‘C6x processors. A value written to it on one memory page is written to the corresponding bit in all other pages.

Important! This bit ***must*** be set to ‘1’ before the mapped HPI memory pages can be used to access the ‘C6x processor memory.

DSPINT Generates an interrupt to the ‘C6x and sets the appropriate bit in the processor node’s **HPI Interrupt** register. It also indicates the state of the DSP interrupt when read. This bit is global for all memory pages. In other words, it will indicate if an interrupt was generated even if read from another memory page register set. Read/Write.

- To generate an interrupt to the ‘C6x, set this bit to ‘1’. (An interrupt is not generated if the bit is already set to ‘1’ before being written.)

The ‘C6x can read the **HPI Interrupt** register to determine which memory page generated the interrupt.

HINT Monitors and clears the HINT interrupt from the DSP to the host system. Read/Write.

- If this bit is ‘1’, then the HINT interrupt from the DSP to the host is active.
- To clear the HINT interrupt, write ‘1’ to this bit.

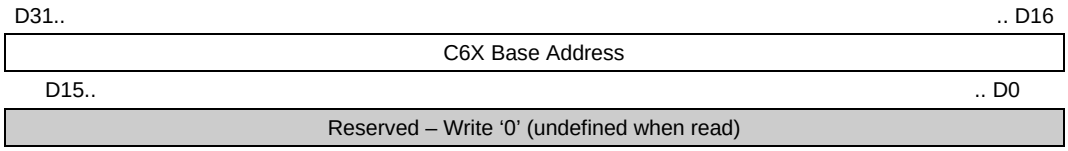
HRDY Indicates whether the HPI is busy. Read-only.

- If this bit is ‘0’, then the host port is busy and cannot transfer data.
- If this bit is ‘1’, then the host port is ready to transfer data.

FETCH Not used. Must be set to ‘0’.

HPI Address Register

Address offsets from the PCI base address 0 (BAR0) of Hurricane X for the memory pages on each node								
Node	**Page 0**	**Page 1**	**Page 2**	**Page 3**	**Page 4**	**Page 5**	**Page 6**	**Page 7**
A	0x00C0 0004	0x00C1 0004	0x00C2 0004	0x00C3 0004	0x00C4 0004	0x00C5 0004	0x00C6 0004	0x00C7 0004
B	0x00C8 0004	0x00C9 0004	0x00CA 0004	0x00CB 0004	0x00CC 0004	0x00CD 0004	0x00CE 0004	0x00CF 0004



Maps the corresponding mapped HPI page to a location within the node's 'C6x processor. The register sets the byte address in 'C6x memory space for the base address of the particular 64K memory page.

Note: The base address must be aligned to a 64K byte address boundary.

Bits D[31..16] contain the base address within the 'C6x for the 64K window. They represent the upper 'C6x address bits D[31..16]. The lower address D[15..0] come from the lower address bits on the PCI address bus. Because the HPI port is word (32-bit) addressed, the lower 2 bits (D[1..0]) of the PCI address are set to '0' when added to the 'C6x base address.

The following figure shows how this register is used for address translation.

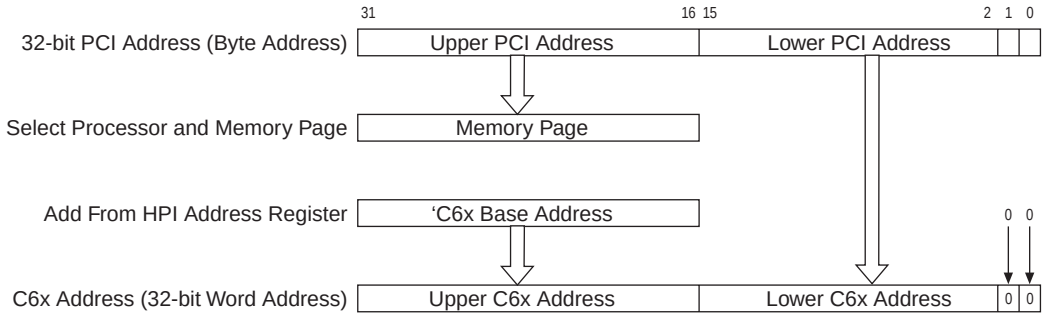
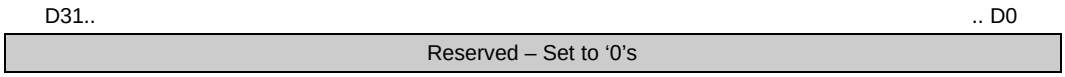


Figure 24 PCI Address to C6x Memory Address Translation

HPI Mode Register

Address offsets from the PCI base address 0 (BAR0) of Hurricane X for the memory pages on each node								
Node	**Page 0**	**Page 1**	**Page 2**	**Page 3**	**Page 4**	**Page 5**	**Page 6**	**Page 7**
A	0x00C0 0010	0x00C1 0010	0x00C2 0010	0x00C3 0010	0x00C4 0010	0x00C5 0010	0x00C6 0010	0x00C7 0010
B	0x00C8 0010	0x00C9 0010	0x00CA 0010	0x00CB 0010	0x00CC 0010	0x00CD 0010	0x00CE 0010	0x00CF 0010



Although this register is not used, it is kept for future compatibility. Do not write any value except 0x0000 0000 to this register.

HPI Interrupt Status Register

Address offsets from the PCI base address 0 (BAR0) of Hurricane X for the memory pages on each node								
Node	**Page 0**	**Page 1**	**Page 2**	**Page 3**	**Page 4**	**Page 5**	**Page 6**	**Page 7**
A	0x00C0 0014	0x00C1 0014	0x00C2 0014	0x00C3 0014	0x00C4 0014	0x00C5 0014	0x00C6 0014	0x00C7 0014
B	0x00C8 0014	0x00C9 0014	0x00CA 0014	0x00CB 0014	0x00CC 0014	0x00CD 0014	0x00CE 0014	0x00CF 0014

D31..							.. D8
Reserved – Set to ‘0’s							
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	ISTAT	0

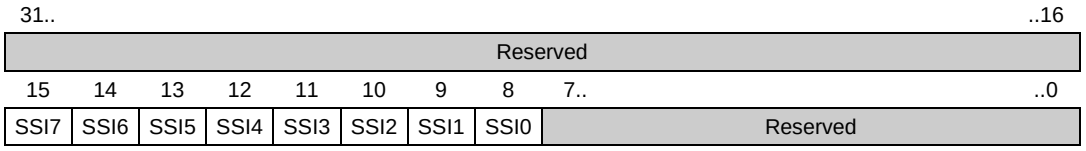
Indicates that the HPI interrupt for the memory page is set. The host system can use this register to determine if the DSP has serviced the interrupt and cleared the interrupt latch. This bit reflects the state of the corresponding HINT(x) bit in the **HPI Interrupt Register** read by the DSP.

ISTAT Interrupt status for the HPI memory page. Read-only.

- When set to ‘1’, the HPI interrupt for this page is active.

SSI Interrupt Register

Node A Hurricane BAR0 address + 0x0018 0000
Node B Hurricane BAR0 address + 0x0018 0000



This register allows any master on the local PCI bus to generate an HPI interrupt on the ‘C6x. The register consists of eight interrupt bits. Writing a ‘1’ to any of these bits generates an HPI interrupt on the ‘C6x. The register can be used by software applications for interrupt-driven messaging involving data transfers to the node’s SSRAM.

SSI[0..7] Generates an HPI interrupt to the ‘C6x through the local DSP Hurricane. One of eight bits can be set to generate the interrupt. The register can also be read to determine which of these interrupts has been set.

Bit	Read	Write
1	SSI(x) latch set	Generates HPI interrupt
0	SSI(x) latch not set	No effect

The DSP reads its **HPI Interrupt** register, at DSP address 0x0170 0000, to identify which SSI latch was set by the interrupt. It can also clear the latch through its **HPI Interrupt** register.

10 DSP Addressable Registers

Each processor node has its own set of registers which are described in this section. These registers are only accessible by their own ‘C6x processor. The registers are summarized in the following table.

Table 14 Processor Node Register Summary

Register	‘C6x Address	Description
HPI Interrupt	0x0170 0000	Identifies HPI interrupt sources
Reserved	0x0170 0004	
Back-off	0x0170 0008	Forces ‘C6x Hurricanes off the local bus
PEM Interrupt Control	0x0170 000C	Enables and routes PEM interrupts
PMC Interrupt Status	0x0170 0010	Monitors and clears PMC interrupts
PMC Interrupt Control	0x0170 0014	Enables PMC interrupts
DSP~LINK3 Interrupt Status	0x0170 0018	Monitors and clears DSP~LINK3 interrupts
DSP~LINK3 Control	0x0170 001C	Controls the DSP~LINK3 interface
Global Interrupt Select	0x0170 0020	Routes and enables global interrupts
Global Interrupt	0x0170 0024	Generates global interrupts
LED	0x0170 0028	Controls the user LEDs
Refresh	0x0170 0030	Enables external refresh requests

HPI Interrupt Register

'C6x address 0x0170 0000

D31..							..D16
Reserved							
D15	D14	D13	D12	D11	D10	D9	D8
SSI7	SSI6	SSI5	SSI4	SSI3	SSI2	SSI1	SSI0
D7	D6	D5	D4	D3	D2	D1	D0
HINT7	HINT6	HINT5	HINT4	HINT3	HINT2	HINT1	HINT0

Indicates the source of a Host Port Interface (HPI) interrupt. There are two methods of generating 'C6x HPI interrupts on the Daytona. Each method has 8 different sources.

- Interrupts generated by setting the DSPINT bit of the **HPI Control** register for a mapped HPI memory page. There are eight pages which are configured by the Hurricane X . These memory page windows are accessed via the 'C6x HPI.
- Interrupts set by the **SSI Interrupt** register for DSP A or DSP B. This register is accessed via the processor node Hurricane. Eight interrupt bits (SSI[0..7]) can be set by any device from the Daytona's local PCI bus.

HINT(x) Reads and clears the HPI interrupt latches corresponding to the eight 'C6x memory pages accessible to the Hurricane X. (x) indicates which of 'C6x memory pages is associated with the interrupt.

Bit	Read	Write
1	HINT(x) latch set	Clears HINT(x) interrupt latch
0	HINT(x) latch not set	No effect

SSI(x) Reads and clears the HPI interrupt latches set through the local DSP Hurricane. The (x) indicates which of SSI Interrupts has been set in the **SSI Interrupt** register for DSP A or DSP B.

Bit	Read	Write
1	SSI(x) latch set	Clears SSI(x) interrupt latch
0	SSI(x) latch not set	No effect

Upon receiving an HPI interrupt, the 'C6x can read this register to determine the source of that interrupt, and then clear it.

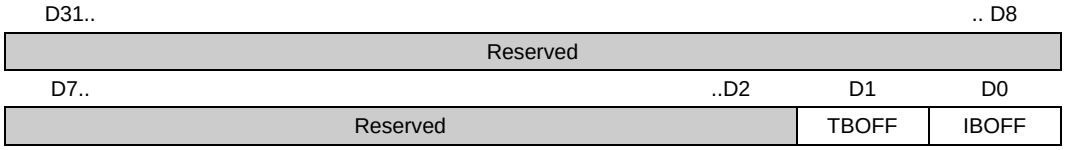
The HPI controller will generate an HPI interrupt if any interrupt bits remain set after a processor has written to the **HPI Interrupt Register**. This ensures that interrupt events are not missed when multiple interrupts are set within the register when an interrupt

service routine has only cleared one of the bits, leaving the remaining bits active. Because the HPI controller detects these active interrupt bits after each write to the regiser, another HPI interrupt is generated. This happens until all interrupt bits in the **HPI Interrupt Register** are cleared.

These interrupts allow software applications to use interrupt-driven messaging for data transfers involving the DSP's memory space or external SSRAM.

Back-off Register

‘C6x address 0x0170 0008



Forces the ‘C6x’s Hurricane off the local bus in response to a DSP~LINK3 interrupt or when the TOUT0 timer pin is driven low.

IBOFF Forces the Hurricane off the local bus when an enabled DSP~LINK3 interrupt goes active low. The DSP~LINK3 interrupts are enabled through the **DSP~LINK3 Control Register** of processor node A. Hurricane is held off the bus until the DSP~LINK3 interrupt is de-asserted. The IBOFF bit applies only to node A. (Read/Write)

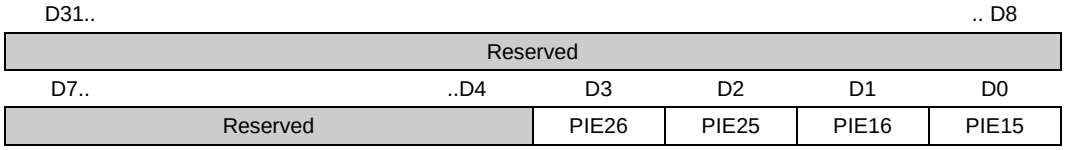
- To force the Hurricane off the local bus upon DSP~LINK3 interrupts, set this bit to ‘1’.
- Upon reset this bit is automatically set to ‘0’

TBOFF Forces the Hurricane off the local bus when the ‘C6x TOUT0 pin goes low. (Read/Write)

- To force the Hurricane off the local bus when TOUT0 goes low, set this bit to ‘1’.
- Upon reset this bit is automatically set to ‘0’

PEM Interrupt Control Register

‘C6x address 0x0170 000C



Enables and routes the two PEM interrupts (PEM INT1 and PEM INT2) to the ‘C6x interrupt pins. Each interrupt has two corresponding bits in the register to PMC interrupts that enables it on EINT5 or EINT6 of the ‘C6x.

- To route an interrupt to a particular ‘C6x interrupt pin (EINT5 or EINT6), set the appropriate bit to ‘1’.
- Upon reset, all bits are automatically set to ‘0’; disabling PEM interrupts to the ‘C6x.

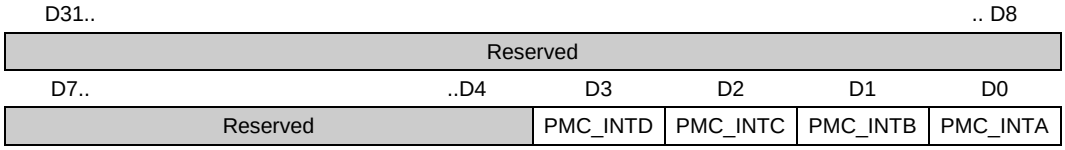
The bit positions for the PEM interrupts and ‘C6x interrupt pins are shown in the following table:

PEM Interrupt	EINT5	EINT6
INT1	PIE15 (D0)	PIE16 (D1)
INT2	PIE25 (D2)	PIE26 (D3)

Note: The PEM interrupts are not latched and the status of the PEM interrupts cannot be directly detected. Interrupt status should be provided by the PEM module. Both PEM interrupts (INT1 and INT2) can be routed to the same ‘C6x interrupt pin (EINT5 or EINT6). Interrupts delivered in this configuration are the logical OR of INT1 and INT2.

PMC Interrupt Status Register

‘C6x address 0x0170 0010



Indicates and clears the status of the PMC interrupt latches. When enabled, a PMC interrupt generates an interrupt on the ‘C6x EINT6 pin. This register indicates which PMC interrupt was the source and allows it to be cleared. Each of the four PMC interrupts (INTA, INTB, INTC, and INTD) has a corresponding bit in the register.

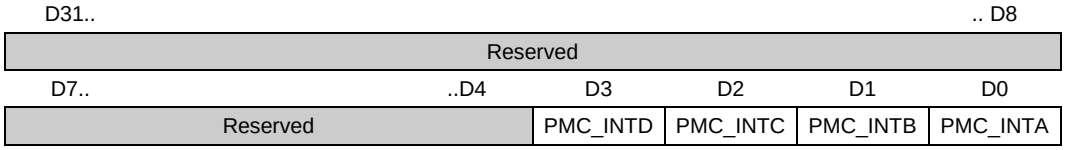
- A ’1’ indicates that the corresponding PMC interrupt has been latched. (Read)
- Writing a ‘1’ to the same bit clears the interrupt latch. (Write)

Although PMC interrupts are defined as level-sensitive interrupts, ‘C6x interrupts are edge sensitive. When the high-to-low transition of an enabled PMC interrupt is latched, a pulse is generated on the ‘C6x EINT6 pin.

Only interrupts that are specified in the write cycle are cleared when writing to the **PMC Interrupt Status** register. If any interrupt latch remains active, another pulse is generated on EINT6.

PMC Interrupt Control Register

‘C6x address 0x0170 0014



Enables any of the four PMC interrupts (INTA, INTB, INTC, and INTD) to generate a low-to-high transition on the ‘C6x interrupt pin EINT6. Each of the four PMC interrupts has a corresponding bit in the register, allowing it to be enabled.

- Writing a ‘1’ to a bit enables high-to-low transitions to be generated on pin EINT6 for the corresponding PMC interrupt.
- Writing a ‘0’ to a bit disables PMC interrupts from EINT6 for the corresponding PMC interrupt.

This register can also be read to determine how the interrupt mask is set. All bits are set to ‘0’ upon reset, disabling all PMC interrupts from reaching EINT6.

DSP~LINK3 Interrupt Status Register

Node A ‘C6x address 0x0170 0018 (reserved for node B)

D31..	.. D8
Reserved	

D7..	..D4	D3	D2	D1	D0
Reserved		DL3_INT3	DL3_INT2	DL3_INT1	DL3_INT0

Indicates and clears the status of the DSP~LINK3 interrupt latches. When enabled, a DSP~LINK3 interrupt generates an interrupt on the ‘C6x EINT5 pin. This register indicates which DSP~LINK3 interrupt was the source and allows it to be cleared. Each of the four DSP~LINK3 interrupts (INT0, INT1, INT2, and INT3) has a corresponding bit in the register.

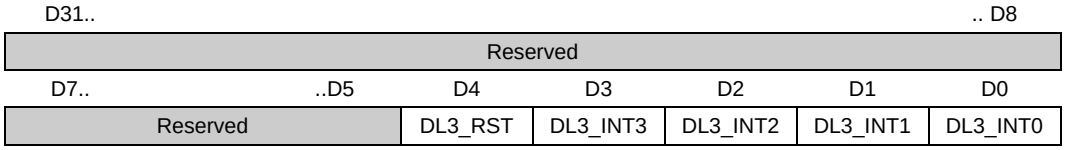
- A ’1’ indicates that the corresponding DSP~LINK3 interrupt has been latched. (Read)
- Writing a ‘1’ to the same bit clears the interrupt latch. (Write)

Although DSP~LINK3 interrupts are defined as level-sensitive interrupts, ‘C6x interrupts are edge sensitive. When the high-to-low transition of an enabled DSP~LINK3 interrupt is latched, a pulse is generated on the ‘C6x EINT5 pin.

Only interrupts that are specified in the write cycle are cleared when writing to the **DSP~LINK3 Interrupt Status** register. If any interrupt latch remains active, another pulse is generated on EINT5.

DSP~LINK3 Control Register

Node A‘C6x address 0x0170 001C (reserved for node B)



Controls the DSP~LINK3 interface on DSP node A.

DL3_INT0, DL3_INT1, DL3_INT2, DL3_INT3 Enables any of the four DSP~LINK3 interrupts (INT0, INT1, INT2, and INT3) to generate a low-to-high transition on the ‘C6x interrupt pin EINT5. Each of the four DSP~LINK3 interrupts has a corresponding bit, allowing it to be enabled.

- Writing a ‘1’ to a bit enables high-to-low transitions to be generated on pin EINT5 for the corresponding DSP~LINK3 interrupt.
- Writing a ‘0’ to a bit disables DSP~LINK3 interrupts from EINT5 for the corresponding DSP~LINK3 interrupt.

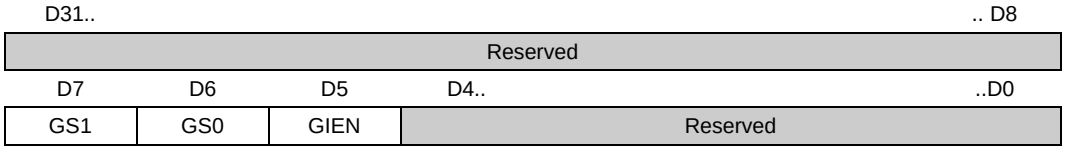
These bits can also be read to determine how the interrupt mask is set. All bits are set to ‘0’ upon reset, disabling all DSP~LINK3 interrupts from reaching EINT5.

DL3_RST Resets the DSP~LINK3 interface.

- To reset the DSP~LINK3 interface set this bit to ‘1’
- Upon Daytona reset, this bit is automatically set to ‘1’; resetting the DSP~LINK3 interface.

Global Interrupt Select Register

Global Interrupt Select Register‘C6x address 0x0170 0020



Routes and enables one of the four global interrupts (GINT0, GINT1, GINT2, and GINT3) to EINT7 of the ‘C6x. The Daytona global interrupts support DSP to DSP, DSP to remote device, and remote device to DSP signaling.

GIEN Enables the interrupt set by the GS1 and GS0 bits.

- To enable the interrupt, set this bit to ‘1’.
- To disable the interrupt and hold EINT7 low, set this bit to ‘0’.

This bit is set to ‘0’, interrupt disabled, upon Daytona reset.

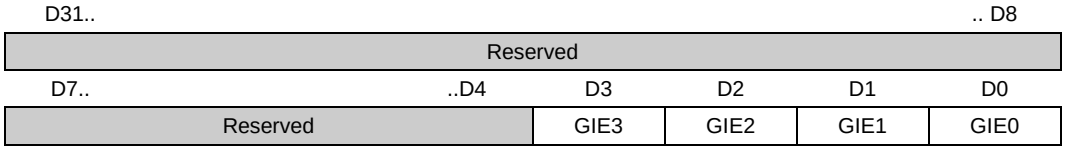
GS1, GS0 These bits select which global interrupt is routed to EINT7 of the ‘C6x according to the following table.

GS1	GS0	Global Interrupt
0	0	GINT0
0	1	GINT1
1	0	GINT2
1	1	GINT3

Upon Daytona reset these bits are set to ‘0’ (GINT0 selected).

Global Interrupt Register

‘C6x address 0x0170 0024



Controls the four global interrupts (GINT0, GINT1, GINT2, and GINT3). The Daytona global interrupts support DSP to DSP, DSP to remote device, and remote device to DSP signaling. The ‘C6x can use this register to drive one or more global interrupts and to get the global interrupt status. Each global interrupt has a corresponding bit in the register.

- To drive a global interrupt low, set its bit to ‘1’.

The interrupts are not affected when their bits are set to ‘0’. Upon reset of the Daytona, these bits are all set to ‘0’.

Note: A DSP node can generate active-low interrupts for either level-sensitive devices or a (high-to-low) edge triggered device using this register.

LED Register

'C6x address 0x0170 0028

	D31..			.. D8
	Reserved			
	D7..	..D2	D1	D0
Node A	Reserved		LED 1	LED 0
Node B	Reserved		LED 3	LED 2

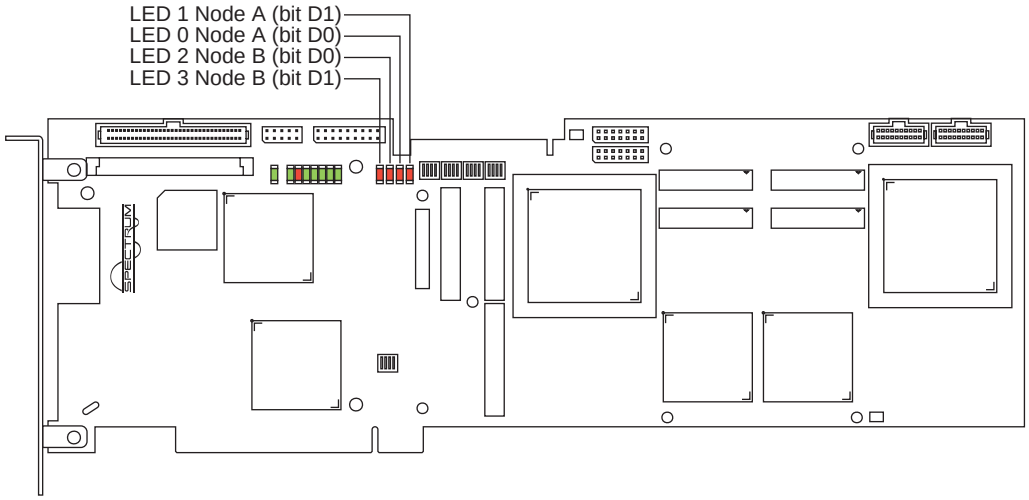
Controls the two user LEDs of each 'C6x node on the Daytona. The LEDs are intended for user diagnostic functions and status reporting. Each LED is controlled by a corresponding bit in this register.

Note: Each 'C6x drives two of the four LEDs on the Daytona board; DSP A drives LEDs 0 and 1, while DSP B drives LEDs 2 and 3.

- To turn an LED on, set its corresponding bit to '1'.
- To turn an LED off, set its corresponding bit to '0'.

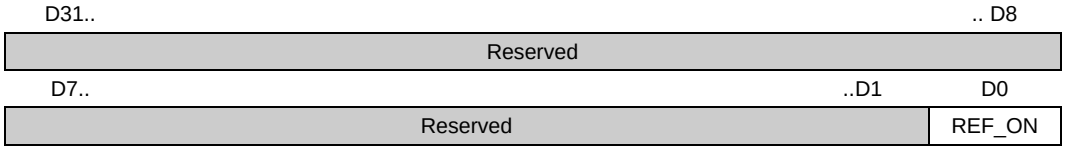
Upon reset of the Daytona these bits are automatically set to '0' (LEDs are turned off).

The following figure shows the user-defined LEDs with their corresponding processors and control bits within this register.



Refresh Register

'C6x address x0170 0030



Enables external refresh requests. Generally, this bit should be left enabled (set to 1). It is used by Daytona software drivers during configuration of the 'C6x EMIF (External Memory Interface) to prevent conflicts caused by external HOLD requests.

- To enable external refresh requests, set the REF_ON bit (D0) to 1.
- To disable external refresh requests, set the REF_ON bit (D0) to 0.

Upon reset, the REF_ON bit (D0) is set to 1.

Custom software drivers that configure the EMIF can use this register to disable refresh requests while the GCR, CE0, CE1, CE2, CE3, and SDRAM interfaces are being configured. An EMIF configuration phase using this register could consist of the following sequence of steps:

1. Set up CE1 memory space timing to allow writes to the register in the next step
2. Write 0x0000 0001 to the **Refresh register** to disable refresh requests
3. Wait 50 ms
4. Set up GCR (disables NOHOLD)
5. Set up CE0 to CE3 values
6. Configure SDRAM
7. Wait 50 ms
8. Write 0x0000 0000 to the **Refresh register** to enable refresh requests

11 Specifications

11.1. Board Identification

Power, current, and data throughput specifications depend upon the type and version of processors used on the board.

Daytona (TMS320C6201B) Current Daytona boards use the TMS320C6201B.

Daytona (TMS320C6201) Earlier Daytona boards use the TMS320C6201.

Daytona67 Daytona67 boards use the TMS320C6701.

The processor type and version can be identified by examining the DSPs on the board.

The board's part number may also be used to determine which DSPs are used on the board. The following table lists Daytona part numbers available at the time this manual was printed.

TMS320C6201 (200 MHz)	TMS320C6201B (200 MHz)	TMS320C6701 (167 MHz)
600-00058	600-00274	600-00252
600-00061	600-00275	600-00253

11.2. General

The Daytona is electrically compliant with PCI Specification Rev 2.1 for 5 Volt cards.

Table 15 Specifications

	Processors			
Parameter	TMS320C6201	TMS320C 6201B	TMS320C6701	Units
Current Consumption	4.88	3.6	4.2	Amps
Power	24.4	18	21	Watts
Supply Voltage (DC)	5			Volts
Operating Temperature	0° to 50°			Celsius

The Daytona is a PCI standard +5 Volt card. On-board power converters generate any other supply voltages required by the board.

11.3. Theoretical Maximum Data Transfer Rates

All values are peak *theoretical* performances.

Source	Target	DSP Clock Speed		Units	Comment
		167 MHz	200 MHz		
‘C6x	SSRAM	334	400	MB/s	
	SDRAM	334	400	MB/s	256 word burst transfer rate
	PEM (SDRAM)	334	400	MB/s	256 word burst transfer rate
Local Hurricane	SSRAM (read)	105		MB/s	
	SSRAM (write)	160		MB/s	Burst rate only. Sustained transfer rates are limited by the PCI bus bandwidth (132 MB/s)
Hurricane X	HPI	>10		MB/s	

11.4. Physical

The Daytona board adheres to the mechanical PCI specifications version 2.1 except for the PCI bracket specification. This difference is shown in the following diagram.

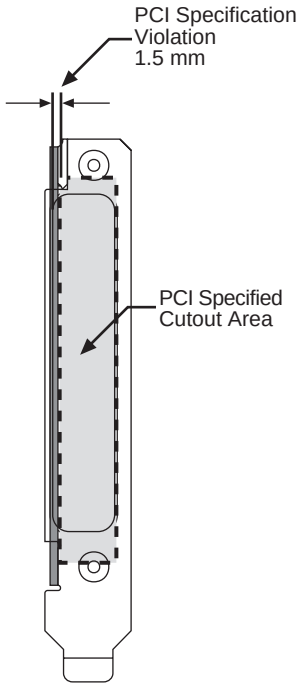
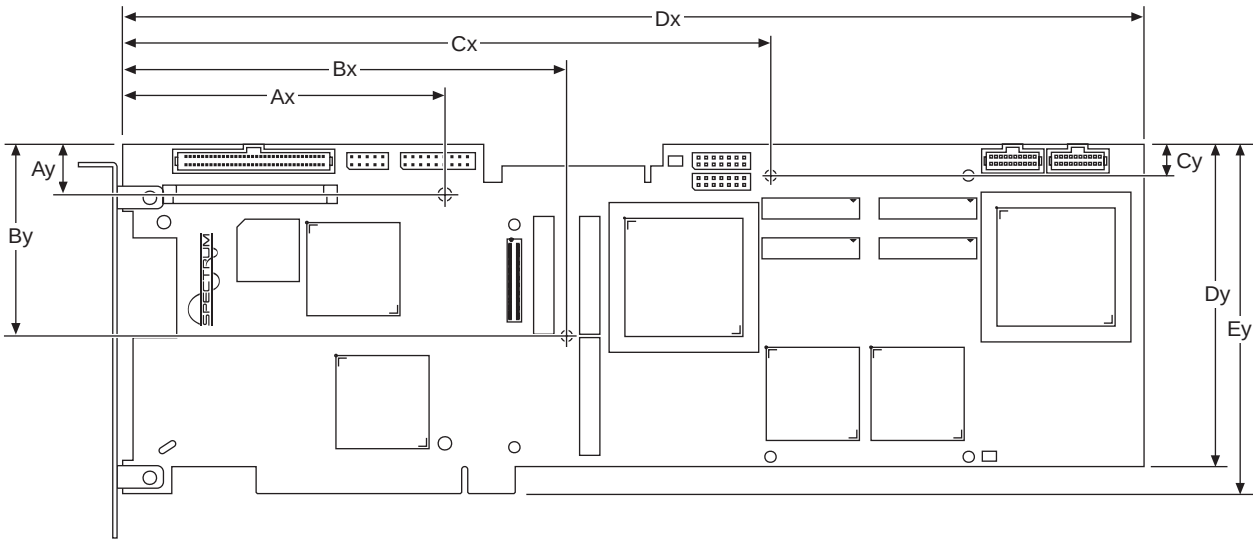


Figure 25 PCI Bracket Dimensions

The DSP~LINK3, PEM, and PMC module sites fully comply with their respective specifications. Exact locations of these modules on the Daytona can be determined using the following diagram and the module's specifications. A location is given (with respect to the upper left corner of the Daytona) for one of the mounting posts for each of the modules. Contact Spectrum Technical Support for more detailed mechanical drawings.



Module	X	Y	Legend
DSP~LINK3	3.880 in	0.600 in	A
PMC	5.341 in	2.303 in	B
PEM	7.773 in	0.375 in	C
Daytona	12.283 in	3.875 in	D
	-	4.200 in	E

Figure 26 Module Locations and Board Dimensions

12 Connector Pinouts

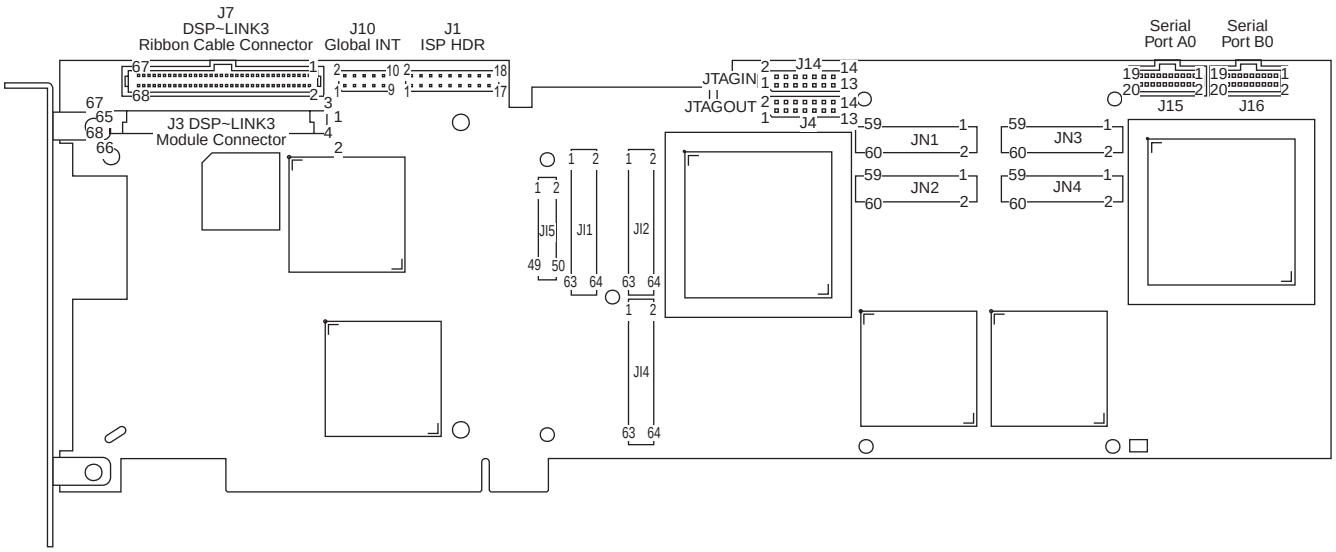


Figure 27 Connector Locations

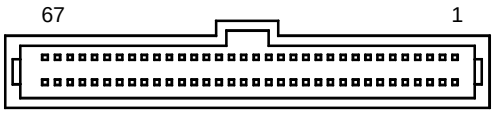
12.1. PCI Card Edge Connector

A standard 120 pin Card Edge Connector provides the interface to the PCI bus. It is keyed as a 5 Volt, 32-bit PCI card. The pin assignment is fully compliant with the *PCI Local Bus Specification.*

12.2. DSP~LINK3 Connectors

Connector pinouts for the DSP~LINK3 module and ribbon cable connectors are given in the following tables. Refer to the *DSP~LINK3 Specification* for complete information.

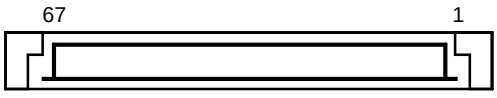
Table 16 DSP~LINK3 Ribbon Cable Connector Pinout (J7)



AMP 1-104068-8

Pin Number	Signal	Pin Number	Signal
1	VCC 1	2	A15
3	A14	4	A13
5	A12	6	A11
7	A10	8	A9
9	A8	10	A7
11	A6	12	A5
13	A4	14	A3
15	A2	16	A1
17	A0	18	R/W_
19	/RESET	20	GND
21	/DSTRB	22	GND
23	/ASTRB	24	GND
25	/RDY	26	GND
27	/INT0	28	GND
29	/INT1	30	GND
31	/INT2	32	GND
33	/INT3	34	GND
35	D31	36	D30
37	D29	38	D28
39	D27	40	D26
41	D25	42	D24
43	D23	44	D22
45	D21	46	D20
47	D19	48	D18
49	D17	50	D16
51	D15	52	D14
53	D13	54	D12
55	D11	56	D10
57	D9	58	D8
59	D7	60	D6
61	D5	62	D4
63	D3	64	D2
65	D1	66	D0
67	GND	68	RSVD

Table 17 DSP~LINK3 Module Connector Pinout (J3)



Hirose FX4C3-68S-1.27DSA

Pin Number	Signal	Pin Number	Signal
1	VCC (+5 V)	35	A15
2	A14	36	A13
3	A12	37	A11
4	A10	38	A9
5	A8	39	A7
6	A6	40	A5
7	A4	41	A3
8	A2	42	A1
9	A0	43	R/W_
10	/RESET	44	GND
11	/DSTRB	45	GND
12	/ASTRB	46	GND
13	/RDY	47	GND
14	/INT0	48	/INT2
15	/INT1	49	/INT3
16	D31	50	D30
17	D29	51	D28
18	D27	52	D26
19	D25	53	D24
20	D23	54	D22
21	D21	55	D20
22	D19	56	D18
23	D17	57	D16
24	D15	58	D14
25	D13	59	D12
26	D11	60	D10
27	D9	61	D8
28	D7	62	D6
29	D5	63	D4
30	D3	64	D2
31	D1	65	D0
32	RSVD	66	RSVD
33	VCC (+5 V)	67	VCC (+5 V)
34	+12 V (unfiltered)	68	-12 V (unfiltered)

12.3. PMC Connector

The PMC connectors use a standard CMC style 1mm pitch SMT connector (AMP 120521-1).

Table 18 PMC Connector JN1

Pin #	Signal	Pin #	Signal
1	TCK	2	-12V
3	GND	4	INTA#
5	INTB#	6	INTC#
7	BMODE1#	8	+5V
9	INTD#	10	RSVD
11	GND	12	RSVD
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	+5V
19	V(I/O)	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	BE3#
27	AD22	28	AD21
29	AD19	30	+5V
31	V(I/O)	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5V
39	GND	40	LOCK#
41	SDONE#	42	SBO#
43	PAR	44	GND
45	V(I/O)	46	AD15
47	AD12	48	AD11
49	AD9	50	+5V
51	GND	52	BE0#
53	AD6	54	AD5
55	AD4	56	GND
57	V(I/O)	58	AD3
59	AD2	60	AD1
61	AD0	62	+5V
63	GND	64	REQ64#

Table 19 PMC Connector JN2

Pin #	Signal	Pin #	Signal
1	+12V	2	TRST#
3	TMS	4	TDO
5	TDI	6	GND
7	GND	8	RSVD
9	RSVD	10	RSVD
11	BMODE2#	12	+3.3V
13	RST#	14	BMODE3#
15	+3.3V	16	BMODE4#
17	RSVD	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3V
25	IDSEL	26	AD23
27	+3.3V	28	AD20
29	AD18	30	GND
31	AD16	32	BE2#
33	GND	34	RSVD
35	TRDY#	36	+3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3V	42	SERR#
43	BE1#	44	GND
45	AD14	46	AD13
47	GND	48	AD10
49	AD8	50	+3.3V
51	AD7	52	RSVD
53	+3.3V	54	RSVD
55	RSVD	56	GND
57	RSVD	58	RSVD
59	GND	60	RSVD
61	ACK64#	62	+3.3V
63	GND	64	RSVD

Table 20 PMC Connector JN4

Pin #	Signal	Pin #	Signal
1	CT_MC	2	CT_D15
3	CT_D14	4	CT_D13
5	CT_D12	6	GND
7	CT_D11	8	CT_D10
9	CT_D9	10	CT_D8
11	CT_D7	12	GND
13	CT_D6	14	CT_D5
15	CT_D4	16	CT_D3
17	CT_D2	18	CT_D1
19	GND	20	CT_D0
21	CLKFAIL	22	/FR_COMP
23	CT_NETREF_1	24	SCLK*
25	GND	26	SCLK-D*
27	SL-4*	28	CLKFAILA*
29	SL-2*	30	SL-3*
31	SL-0*	32	SL-1*
33	/CT_RESET	34	CT_D16
35	/CT_EN	36	CT_D17
37	/CT_FRAME_A*	38	CT_D18
39	GND	40	CT_D19
41	/CT_FRAME_B*	42	CT_D20
43	GND	44	CT_D21
45	CT_C8_A	46	CT_D22
47	GND	48	CT_D23
49	CT_C8_B	50	CT_D24
51	GND	52	CT_D25
53	CT_NETREF_2*	54	CT_D26
55	reserved*	56	CT_D27
57	reserved*	58	CT_D28
59	reserved*	60	CT_D29
61	reserved*	62	CT_D30
63	reserved*	64	CT_D31

*The shaded connections are not physically connected on the Daytona.

This connector is used to route the synchronous serial ports from each DSP to a non-standard PMC module (AMP 5-316466-0)

Table 21 Non-standard PMC Connector JN5

Pin #	Signal	Pin #	Signal
1	CLKS1_A	3	CLKS1_C
3	GND	4	GND
5	CLKR1_A	6	CLKR1_C
7	GND	8	GND
9	CLKX1_A	10	CLKX1_C
11	DR1_A	12	DR1_C
13	DX1_A	14	DX1_C
15	FSR1_A	16	FSR1_C
17	FSX1_A	18	FSX1_C
19	GND	20	GND
21	CLKS1_B	22	CLKS1_D
23	GND	24	GND
25	CLKR1_B	26	CLKR1_D
27	GND	28	GND
29	CLKX1_B	30	CLKX1_D
31	DR1_B	32	DR1_D
33	DX1_B	34	DX1_D
35	FSR1_B	36	FSR1_D
37	FSX1_B	38	FSX1_D
39	GND	40	GND
41	reserved	42	reserved
43	SCLK	44	SCLKX2
45	C2	46	CT_C8_B
47	/C4	48	CT_C8_A
49	C16	50	/C16

12.4. JTAG Connectors

JTAG connection is provided by a pair of 0.1” by 0.1” grid 14-pin header connectors (AMP 103186-10). One for JTAG OUT, and one for the JTAG IN which are located on the Daytona.

Table 22 JTAG IN Connector (J14)

Pin Number	Signal	Pin Number	Signal
1	TMS	2	/TRST
3	TDI	4	GND
5	Presence Detect (+3.3V)	6	Pin Missing
7	TDO	8	GND
9	TCK_RET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1

Table 23 JTAG OUT Connector (J4)

Pin Number	Signal	Pin Number	Signal
1	TMS	2	/TRST
3	TDO	4	GND
5	SENSE	6	N/C
7	TDI	8	GND
9	TCK_RET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1

12.5. ‘C6x Serial Port Connectors

Two 20-pin connectors (AMP 104068-1) provide direct access to the serial ports of the ‘C6x. Note the following for each connector:

- The same CLKSx signal appears on both pin 7 and 14.
- Some signals are shown as *TDM*/*Standard* format. For example, TCLK/CLKX0 (pin 1) is TCLK in TDM mode, CLKX0 in standard mode.

Table 24 DSP A Serial Port 0 Connector (J15)

Pin	TDM/Standard Function	Pin	TDM/Standard Function
1	TCLK/CLKX0	2	GND
3	TFRM/FSX0	4	GND
5	TDAT/DX0	6	GND
7	CLKS0	8	GND
9	GND	10	GND
11	GND	12	GND
13	GND	14	CLKS0
15	GND	16	NC/DR0
17	GND	18	TADD/FSR0
19	GND	20	NC/CLKR0

Table 25 DSP B Serial Port 1 Connector (J16)

Pin	TDM/Standard Function	Pin	TDM/Standard Function
1	TCLK/CLKX1	2	GND
3	TFRM/FSX1	4	GND
5	TDAT/DX1	6	GND
7	CLKS1	8	GND
9	GND	10	GND
11	GND	12	GND
13	GND	14	CLKS1
15	GND	16	NC/DR1
17	GND	18	TADD/FSR1
19	GND	20	NC/CLKR1

12.6. PEM Connectors

Both PEM connectors use 60 pin 0.8 mm pitch SMT connectors (AMP 5-179009-2).

Table 26 PEM 1 Connector Pinout (JI1 and JI3)

Pin #	Signal	Pin #	Signal
1	GEN_CLK	2	GND
3	EA2	4	ED16
5	EA3	6	ED17
7	EA4	8	ED18
9	EA5	10	ED19
11	EA6	12	ED20
13	EA7	14	ED21
15	EA8	16	ED22
17	EA9	18	ED23
19	GND	20	GND
21	EA10	22	ED24
23	EA11	24	ED25
25	EA12	26	ED26
27	EA13	28	ED27
29	EA14	30	ED28
31	EA15	32	ED29
33	EA16	34	ED30
35	EA17	36	ED31
37	+3V	38	+5V
39	+3V	40	+5V
41	EA18	42	CLKX0
43	EA19	44	FSX0
45	/ARE	46	DX0
47	ARDY	48	DR0
49	/PEM_CE1	50	FSR0
51	/AWE	52	CLKR0
53	/AOE	54	GND
55	GND	56	CLKS0
57	SDCLK	58	/RESET
59	GND	60	PEM_INT1

Table 27 PEM 2 Connector Pinout (JI2 and JI4)

Pin #	Signal	Pin #	Signal
1	GND	2	GND
3	CLKX1	4	ED0
5	FSX1	6	ED1
7	DX1	8	ED2
9	DR1	10	ED3
11	FSR1	12	ED4
13	CLKR1	14	ED5
15	GND	16	ED6
17	CLKS1	18	ED7
19	RSVD	20	GND
21	/PEM_CE2	22	ED8
23	RSVD	24	ED9
25	/HOLD	26	ED10
27	/HOLDA	28	ED11
29	RSVD	30	ED12
31	EA20	32	ED13
33	EA21	34	ED14
35	RSVD	36	ED15
37	+3V	38	+5V
39	+3V	40	+5V
41	/BE0	42	DMAC0
43	/BE1	44	DMAC1
45	/BE2	46	DMAC2
47	/BE3	48	+12V
49	/SDRAS	50	-12V
51	/SDCAS	52	PEM_INT2
53	/SDWE	54	RSVD
55	GND	56	GND
57	PEM_TIMER	58	RSVD
59	GND	60	SDA10

12.7. Global Interrupt Header

The four open-collector global interrupt signals are presented on a keyed 2 mm pitch 2x5 header (Harwin M22-2020405).

Table 28 Global Interrupt Connector Pinout

Pin #	Signal	Signal	Pin #
1	/GINT0	GND	2
3	/GINT1	GND	4
5	/GINT2	GND	6
7	/GINT3	GND	8
9	GND	GND	10

Index

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